Analysis of Worst-case of Loss and Crosstalk for Planar Silicon Photonic Switch Architectures

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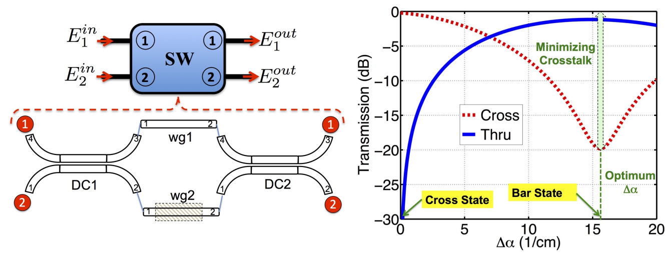
***Abstract*— We discuss the impact of optimal 2×2 Mach-Zehnder switch design and waveguide crossings on the scalability of planar switches in silicon photonics platform. We show the importance of multi-path coherent crosstalk in scalable switch architectures by particularly examining 16×16 Benes and PI-LOSS structures.**

Optical switching can contribute to reduce the many optical/electrical/optical conversions that occur in large datacenters or supercomputers interconnects [1]. Large port count, i.e. large radix, switches in bulk optics based on MEMS are being commercialized already. However, to deploy optical switching at large scale, for example to enable bandwidth steering in a Dragonfly topology [2], more integrated, thus cheaper, optical switches are necessary. The silicon photonics platform has proven a worthy option in terms of performance, but over all in terms of integration, with a fast growth over the last decade [3]. Today, individual broadband silicon photonic switches based on Mach-Zehnder interferometers have been fabricated, tested, and shown to provide fast switching speeds (∼ ns). Calo *et al.* [4] provided a detailed analysis of design and analysis of 2×2 silicon-based electro-optic Mach-Zehnder switch (MZS), concluding that an insertion loss of 1.1 dB, a crosstalk level of -15 dB with an optical bandwidth of 60 nm is achievable. In 2015, Dupuis *et al.* [5] from IBM revisited the concept of 2×2 MZS in silicon photonic platform. Leveraging IBM's 90nm CMOS platform, and optimizing their design for minimal loss and crosstalk, this group proved that insertion loss of 1dB and crosstalk of -23 dB with an optical bandwidth 45nm and 4 ns switching time is possible. Later that year, the same group further introduced these 2×2 MZS as the enabling technologies for fast and scalable silicon photonic switches by demonstrating a 4×4 switch based on 2x2 switches [6]. Other researchers have strived to scale up the port count of larger numbers. For example, in 2016, Lu *et al.* [7] demonstrated a 16x16 non-blocking switch based on Benes topology with a total footprint of 40 mm^2. The measured loss and crosstalk in the "cross state" of the 2x2 MZS were 0.1 dB and -30 dB over a wavelength range of 30nm. In the "bar state" the numbers degraded to 1dB and -18dB, respectively.

In this talk, we first present the modeling of 2×2 MZS in our simulation platform called PhoenixSim [8] and show that its predictions are well aligned with the published devices. As shown in Fig. 1(a) our 2×2 switch consists of two input and output directional couplers and two waveguides that form the arms of the interferometer. The waveguides are assumed standard silicon nano-wires with a cross-section of 450nm×220 nm. Fig. 1(b) shows the electro-optic behavior of the switch in a single-arm operation. The insertion loss and crosstalk are estimated to be 0.2 dB and <-30 dB in the "cross" state, and



(a) (b)

Fig. 1. Schematic of a 2×2 MZI switch with the Cross and Thru states optimized for minimum crosstalk leakage. (a) The physical construction of the 2×2 MZI switch. Two directional couplers and two straight waveguides constitute the switch. (b) Electro-optic response of the 2×2 switch. The cross states and the bar states are marked.

1.2 dB and -19.8 dB in the "bar" state. We will then show how this 2×2 switch element can be used to construct larger switches such as 16×16 Benes and PILOSS switches, and how the loss and crosstalk for each switch configuration is analyzed in our simulation platform. One input port is excited, the light is propagated through the switch fabric, and the optical power at each output port is eventually monitored. Due to the crossing of waveguide connections and finite extinction of each 2×2 switch, coherent multi-path interference is observed for the crosstalk power at each output port.

We will show that considerable variations of both loss and crosstalk are observable within a single switch, depending on the requested switch permutation. A "worst-case performance graph" that maps each input port to each output port based on worst-case of insertion loss and worst-case of crosstalk will be presented for various switch architectures. The influence of waveguide crossings will also be discussed. In light of these results, we will draw conclusions on the potential of MZS based switches in silicon for optical interconnects applications.

References

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