Broadband Operation of Nanophotonic Router for Silicon Photonic Networks-on-Chip

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Abstract—A nonblocking four-port bidirectional multiwavelength message router for use in photonic network-on-chip (NoC) architectures implementing two-dimensional mesh or torus topologies is fully characterized with bit-error-rate measurements and eye diagrams using three wavelength-parallel 10-Gb/s channels. The experiments demonstrate the feasibility of using this advanced switching subsystem within dynamically routed multiwavelength photonic NoCs.

Index Terms—Multiprocessor interconnection, optical resonators, optical switches, photonic switching systems, wavelength-division multiplexing.

I. Introduction

HE increasing number of cores in current chip multiprocessors (CMPs) places a heightened emphasis on the performance of the on-chip communications infrastructure. As a result, conventional electronic wiring will face difficulties providing the required on-chip bandwidths, while remaining within reasonable power constraints. These limitations are aggravated by a growing discrepancy between on- and off-chip bandwidths, which has become more severe over the last two decades due to the power and area required to drive signals off chip using electrical interconnects.

Photonic networks-on-chip (NoCs) introduce a logical solution, since 1) photonic links provide very large bandwidths, methodically scalable with the wavelength parallelism of the optical domain, and 2) photonic messages can be exchanged in a highly energy-efficient manner [1]. Moreover, the equivalent

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power consumption of on- and off-chip photonic signaling makes the on-chip photonic communications infrastructure also beneficial for off-chip memory accesses [2]. Significant advancements in complementary metal—oxide—semiconductor (CMOS)-compatible silicon photonic technologies have provided a viable path toward the realization of photonic NoCs, due to mature processing capabilities and high index contrast, which affords dense photonic integration. Today, all of the necessary components for constructing simple NoCs (e.g., modulators [3], switches [4], [5], receivers [6]) have been demonstrated, and designers currently strive toward obtaining performance improvements and increasing the level of device integration.

In previous work, we have studied electronically controlled circuit-switched photonic NoCs, arranged in a variety of two-dimensional (2-D) topologies [1], [7]. The most prevalent photonic network element in these topologies is the nonblocking four-port bidirectional router, which dynamically routes broadband messages to their target destinations. These networks utilize wavelength-parallel message encoding for optical-domain bandwidth enhancement. That is, multiple wavelength channels are passed through the network from source to destination cohesively, as a combined data-carrying unit, while other messages in the network circumvent contention using spatial avoidance. The network performance in every topology, as expected, has been shown to be vastly improved when multiple multiwavelength messages can simultaneously pass through the photonic routers without contention. Therefore, the routing elements in these topologies must ideally provide four bidirectional input/output (I/O) ports, with multiwavelength routing capabilities and strictly nonblocking functionality. Such a router has been designed, and its network-level performance has been evaluated through simulations [1], [7]. Furthermore, the router was fabricated [8], and initial data characterizations were performed [9], [10]. In this work, we present the router's experimentally verified performance of broadband operation, with a full characterization of multiwavelength single-message routing.

II. NONBLOCKING FOUR-PORT BIDIRECTIONAL ROUTER

The device fabrication of the four-port router was performed at the Cornell Nanofabrication Facility [8]. The router [Fig. 1(a)] consists of both photonic and thermo-electric circuits. Optically, it is composed of waveguides with 450-nm \times 250-nm cross sections, waveguide crossings that are adiabatically tapered to 2- μ m widths at the intersection to minimize reflections, and ring resonators with 20- μ m diameters. The structure provides

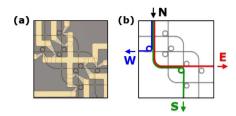


Fig. 1. (a) Microscope image of the fabricated nonblocking four-port bidirectional multiwavelength message router. (b) Schematic of the router, highlighting the signal paths of the three experimental switch configurations: $N \to E, N \to S$, and $N \to W$.

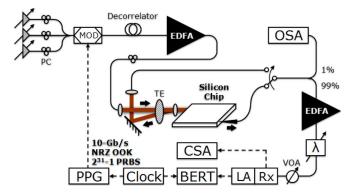


Fig. 2. Diagram of the experimental setup, including the three-beam coupling configuration utilizing free-space optics on one side of the chip and tapered-lensed fiber on the other side. Solid and dashed lines represent optical fiber and electrical cable, respectively.

a dedicated path for every I/O combination except U-turns, which are unnecessary in circuit-switched networks. The router employs the minimum eight ring resonators, each coupled to a waveguide crossing, comprising four 1×2 switches (with a single ring at a crossing) and two 2×2 switches (with two rings at a crossing), similar to those individually demonstrated in [4] and [5], respectively. The electronic heaters provide static switch-state configuration using direct-current (dc) resonance tuning. In this work, we refer to the four router I/O ports as *North* (N), *East* (E), *South* (S), and *West* (W), corresponding to their relative positions.

The experimental setup (Fig. 2) consists of three combined tunable laser sources, with optical powers equalized to 7 dBm, simultaneously modulated with a 10-Gb/s nonreturn-to-zero (NRZ) on-off-keyed (OOK) signal encoded using a pseudorandom bit sequence (PRBS). A 25-km standard single-mode fiber provides adequate decorrelation between the three wavelength channels, and an erbium-doped fiber amplifier (EDFA) amplifies the signals before their injection into the chip. At the output of the chip, part of the extracted signal is monitored on an optical spectrum analyzer (OSA), while the remainder is preamplified using another EDFA, filtered using a tunable grating filter (λ) with a 3-dB bandwidth of 0.22 nm, and received using a high-speed PIN photodiode and transimpedance amplifier (PIN-TIA) receiver. Once received, the signal is evaluated on a communications signal analyzer (CSA), and the error performance is quantified by a bit-error-rate (BER) tester (BERT) after passing through a limiting amplifier (LA).

Single-Channel (1546-nm) Routing Verification for Three Switch Configurations: N→E, N→S, and N→W

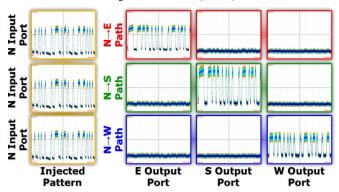


Fig. 3. CSA pattern traces depicting single-channel (1546-nm) verification of the routing functionality for three experimental switch configurations: N \rightarrow E, N \rightarrow S, and N \rightarrow W. In each configuration, a single-wavelength signal (injected pattern) is injected into the North (N) input port, and examined on each output port (E, S, and W). Each trace spans 5 ns and has an amplitude scale of 100 μ W/division, except for the input pattern and the East (E) output pattern under the N \rightarrow E configuration, which are 200 μ W/division. A PRBS pattern with a length of $2^{7}-1$ is used for the pattern traces.

The clock synthesizer synchronizes the pulse pattern generator (PPG) to the BERT. Polarization controllers (PCs) are used throughout the setup.

The waveguides are equipped with inverse-taper mode converters at each chip edge, and at one side of the chip a tapered-lensed fiber is employed to gather light from both the East and South output ports, alternately. At the other side of the chip, a lens is used to collimate light exiting from the West port while simultaneously focusing light entering into the North port. A polarizer transmits the transverse-electric (TE) polarization component of the two collimated beams.

III. RESULTS AND DISCUSSION

Both single- and multiwavelength experiments are performed to demonstrate the operation of the router. Here, the signal that egresses from the East, South, and West output ports is monitored while injecting into the North input port [Fig. 1(b)]. First, pattern traces of the single-channel signal exiting the destination output ports, along with the noise observed on the other output ports, are illustrated in Fig. 3, indicating extinction ratios in excess of 8 dB for each port.

Utilizing three consecutive resonance modes of the ring resonators, which have free-spectral ranges of approximately 8 nm and 3-dB bandwidths of about 38.5 GHz, a three-channel wavelength-parallel signal is then routed through the same switch configurations described above. Recorded eye diagrams for the three-channel signal injected into the North input port, as well as at each destination output port for each experimental switch configuration, are recorded for each of the three 10-Gb/s wavelength channels, which are located at 1538, 1546, and 1554 nm (Fig. 4). Additionally, BER curves are taken for each wavelength channel in each configuration (Fig. 5). The back-to-back curves are also taken on each channel by replacing the chip with a variable optical attenuator (VOA) set to mimic the minimum fiber-to-fiber losses (which are observed for path N \rightarrow E).

Configurations: $N \rightarrow E$, $N \rightarrow S$, and $N \rightarrow W$ Particle Input λ_1 1538 nm 1546 nm 1554 nm Output λ_1 Output λ_2 Output λ_3 Output λ_3

Three-Channel Routing for Three Switch

Fig. 4. The 10-Gb/s eye diagrams for the three-channel input signal (injected signal) injected into the North (N) input port, with eye diagrams for the three-channel output signal at the destination output port, for each experimental switch configuration: $N \to E, \, N \to S,$ and $N \to W.$ The wavelength-parallel signal consists of three 10-Gb/s channels, located at 1538, 1546, and 1554 nm. Each eye diagram has a 200-ps time span. A PRBS pattern with a length of $2^{31}-1$ is used for the eye diagrams.

1546 nm

1554 nm

1538 nm

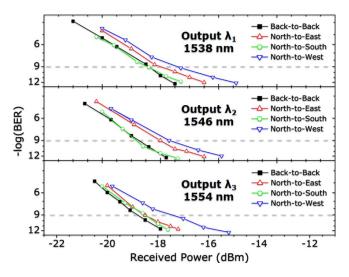


Fig. 5. The 10-Gb/s BER curves quantifying multiwavelength routing signal integrity for the three-channel input signal injected into the North (N) input port, and examined at the destination output port, for each experimental switch configuration: N \rightarrow E, N \rightarrow S, and N \rightarrow W. The wavelength-parallel signal consists of three 10-Gb/s channels, located at 1538, 1546, and 1554 nm. The back-to-back BER curves are taken for configurations bypassing the chip. A PRBS pattern with a length of $2^{31}-1$ is used for the BER measurements.

The power penalties, defined as the degradation in receiver sensitivity incurred by the device under test, are approximately 1.3 dB for the N \rightarrow W state, at the BER of 10^{-9} . Both of the other states demonstrate power penalties below 1 dB for all three wavelength channels.

IV. CONCLUSION

We have experimentally demonstrated and characterized the broadband operation of a nonblocking four-port photonic router with three wavelength-parallel channels, each operating at 10 Gb/s. We have verified appropriate routing functionality for multiwavelength messages exiting all three output ports, and quantified the resulting output signal integrity using eye diagrams and BER characterization, demonstrating the router's feasibility within photonic NoCs for next-generation CMPs.

REFERENCES

- A. Shacham, B. G. Lee, A. Biberman, K. Bergman, and L. P. Carloni, "Photonic NoC for DMA communications in chip multiprocessors," in Proc. 15th Annu. IEEE Symp. High-Performance Interconnects, 2007, pp. 29–36.
- [2] C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. Holzwarth, M. Popović, H. Li, H. Smith, J. Hoyt, F. Kärtner, R. Ram, V. Stojanović, and K. Asanović, "Building manycore processor-to-DRAM networks with monolithic silicon photonics," in *Proc. 16th Annu. IEEE Symp. High-Performance Interconnects*, 2008, pp. 21–30.
- [3] Q. Xu, B. Schmidt, J. Shakya, and M. Lipson, "Cascaded silicon microring modulators for WDM optical interconnection," *Opt. Express*, vol. 14, pp. 9430–9435, 2006.
- [4] B. G. Lee, A. Biberman, P. Dong, M. Lipson, and K. Bergman, "All-optical comb switch for multiwavelength message routing in silicon photonic networks," *IEEE Photon. Technol. Lett.*, vol. 20, no. 10, pp. 767–769, May 15, 2008.
- [5] B. G. Lee, A. Biberman, N. Sherwood-Droz, C. B. Poitras, M. Lipson, and K. Bergman, "High-speed 2 × 2 switch for multiwavelength silicon-photonic networks-on-chip," *J. Lightw. Technol.*, vol. 27, no. 14, pp. 2900–2907, Jul. 15, 2009.
- [6] P. C. P. Chen, A. M. Pappu, and A. B. Apsel, "Monolithic integrated SiGe optical receiver and detector," in *Proc. Conf. Lasers and Electro-Optics, Tech. Dig. (CD) (Optical Society of America)*, Baltimore, MD, 2007, pp. 1–2, Paper CTuZ4.
- [7] H. Wang, M. Petracca, A. Biberman, B. G. Lee, L. P. Carloni, and K. Bergman, "Nanophotonic optical interconnection network architecture for on-chip and off-chip communications," in *Proc. Optical Fiber Communications Conf. (IEEE)*, San Diego, CA, 2008, pp. 1–3, Paper IThA92
- [8] N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, "Optical 4 × 4 hitless silicon router for optical networks-on-chip (NoC)," *Opt. Express*, vol. 16, pp. 15915–15922, 2008.
- [9] A. Biberman, N. Sherwood-Droz, B. G. Lee, M. Lipson, and K. Bergman, "Thermally active 4 × 4 non-blocking switch for networks-on-chip," in *Proc. Annu. Meeting Lasers and Electro-Optics Society (IEEE)*, Newport Beach, CA, 2008, pp. 370–371, Paper TuBB3
- [10] B. G. Lee, A. Biberman, K. Bergman, N. Sherwood-Droz, and M. Lipson, "Multi-wavelength message routing in a non-blocking four-port bidirectional switch fabric for silicon photonic networks-on-chip," in *Proc. Optical Fiber Communications Conf. (IEEE)*, San Diego, CA, 2009, pp. 1–3, Paper OMJ4.