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High-Speed Data Transmission in Multi-Layer Deposited Silicon Photonics for Advanced Photonic Networks-on-Chip

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Abstract: We introduce a multi-layer silicon photonic microring resonator filter, fabricated using deposited materials, and transmit up to 12.5-Gb/s error-free data, establishing a novel class of high-performance silicon photonics for advanced photonic NoCs.

OCIS codes: (130.3120) Integrated optics devices; (200.4650) Optical interconnects

1. Introduction

Advanced silicon photonic devices and systems, constructing photonic networks-on-chip (NoCs), are slated to be instrumental in enabling new generations of computational parallelism leveraging chip multiprocessors (CMPs) and memory access systems [1]. These photonic NoCs have the potential to supply an immense amount of bandwidth, while reducing the total energy consumption. The extent of this vast potential depends on the development and refining of silicon photonic materials, devices, and systems. The silicon-on-insulator (SOI) platform has already enabled many of the key devices, such as waveguides, filters, modulators, and switches [2]. Other CMOS-compatible materials have yielded fundamentally-novel devices such as laser sources [3], ultralow-loss waveguides [4], and photodetectors [5]. Furthermore, recent efforts have delivered high-quality silicon photonic devices based on materials capable of being deposited, including polycrystalline silicon and silicon nitride. Using multi-layer integration, these deposited materials can be combined in ways previously not possible, forming complex photonic integrated circuits (PICs) spanning three dimensions, while simultaneously eliminating in-plane waveguide crossings. This approach allows for the precise tailoring of each device to utilize materials with the most desirable properties.

In this work, we introduce a two-layer device fabricated using high-quality deposited silicon photonics. To the best of our knowledge, the device presented in this work represents the first realized CMOS-compatible multi-layer photonic structure, consisting of two deposited silicon nitride layers surrounded and separated by deposited silicon dioxide layers. The bottom silicon nitride layer comprises a waveguide coupled to a microring resonator, forming an optical filter with a through port (Fig. 3). The 60-µm-diameter microring resonator is also simultaneously vertically coupled to the top silicon nitride layer, comprising another waveguide, providing a drop port to this optical filter (Fig. 3). All of the waveguides are 1-µm wide and 400-nm tall, with about 1-dB/cm propagation losses. All the layers of this device are deposited using plasma-enhanced chemical vapor deposition (PECVD), patterned using i-line photolithography, and planarized using chemical-mechanical polishing (CMP).

2. Experiments and results

The experimental setup (Fig. 1) comprises a tunable laser (TL) source generating CW light, which is modulated (MOD) with a non-return-to-zero on-off-keyed (NRZ-OOK) signal, encoded using a $2^{31}-1$ pseudo-random bit sequence (PRBS) generated by a pulse pattern generator (PPG). The optical signal passes through a fiber polarizer, selecting the quasi-TE propagation mode, and couples into the on-chip nanotapered silicon waveguide using a tapered fiber. Off chip, the optical signal passes through a variable optical attenuator (VOA), before being detected using a high-speed PIN photodiode and transimpedance amplifier (PIN-TIA) receiver and a limiting amplifier (LA). The received data is evaluated using a BER tester (BERT). The PPG and the BERT are synchronized to the same clock source. An optical spectrum analyzer (OSA) and a digital communications analyzer (DCA) are used to evaluate the spectral and temporal performance, respectively. Before the DCA, the optical signal is amplified (EDFA) and filtered (λ). The average optical power injected into the silicon chip is 1.5 dBm. We record the spectral response of this device, observing the resonance spectral profile for both output ports (Fig. 2). We measure a 6.7-nm free-spectral range (FSR), and a modulation depth of 20 and 18.75 dB, for the through and drop port, respectively.

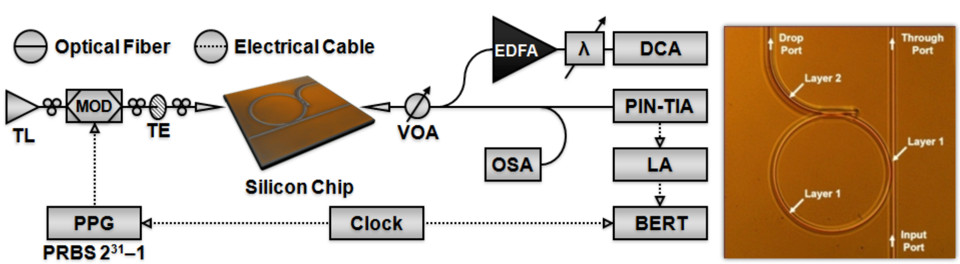

Fig. 1. Diagram of the experimental setup used for BER measurements using the multi-layer silicon photonic microring resonator filter (left), and top-view microscope image of the device (right).

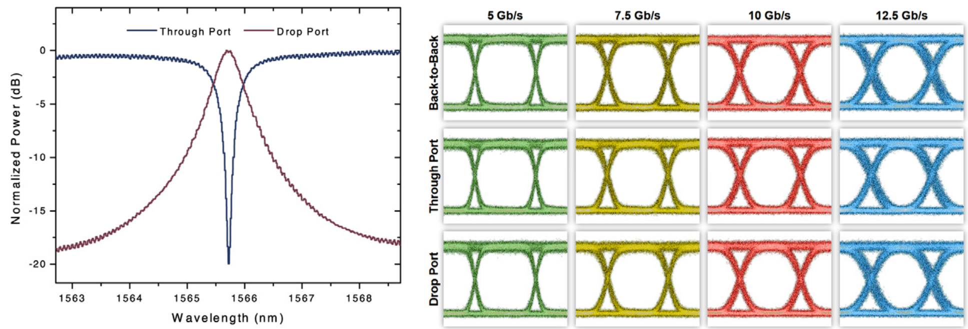

Fig. 2. Spectral response of the multi-layer silicon photonic microring resonator filter for both output ports (left), and output eye diagrams for optical signals with 5-, 7.5-, 10-, and 12.5-Gb/s data rates, egressing from both output ports of the filter, as well bypassing the silicon chip in the back-to-back case (right).

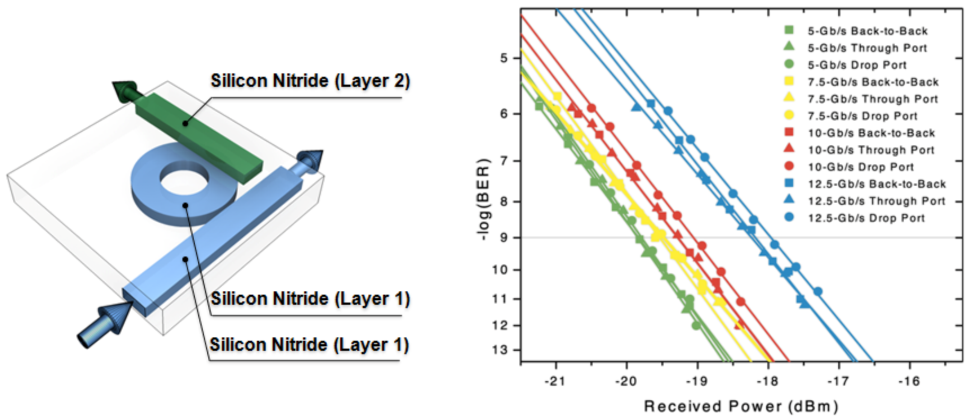

Fig. 3. Three-dimensional schematic representation of the multi-layer silicon photonic microring resonator filter (left), and measured BER curves for optical signals with 5-, 7.5-, 10-, and 12.5-Gb/s data rates, egressing from both output ports of the filter, as well as bypassing the silicon chip in the back-to-back case (right).

By tuning the center wavelength of an incoming high-speed data signal, we select from which output port of the filter the signal will egress. We first inject a high-speed data signal at the input port of the device, setting the center wavelength to 1568.5 nm, and vary the data rate to determine its impact on the resulting signal quality. This signal bypasses the microring resonator, and egresses from the through port of the device, where we record the corresponding eye diagrams for 5, 7.5, 10, and 12.5 Gb/s (Fig. 2). Tuning the center wavelength to 1565.7 toggles the signal to transmit through the microring resonator, and egress from the drop port of the device, where we record the corresponding eye diagrams for the varying data rate (Fig. 2). We compare these eye diagrams with the back-to-back case, where we bypass the silicon chip and replace it with a VOA set to mimic the fiber-to-fiber insertion loss of the device (about 8 dB). We then perform BER measurements for each data rate at each output port of the device. We observe error-free operation (defined as having BERs less than 10^{-12}), and subsequently record the BER curve, for every configuration including the back-to-back case bypassing the silicon chip (Fig. 3). For the through port, the resulting measured power penalties are negligible for every measured data rate up to 12.5 Gb/s. For the drop port, the power penalties are negligible up to 7.5 Gb/s, and are 0.22 and 0.23 dB for 10 and 12.5 Gb/s, respectively. Part of the observed power penalty may be attributed to spectral filtering of the signal sidebands through the microring resonator.

3. Conclusions

We have presented a powerful technique for realizing high-performance multi-layer silicon photonics, with devices methodically scalable to enable unprecedented performance in advanced photonic NoCs. We have verified and characterized the operation of a multi-layer silicon photonic microring resonator filter, operating with high-speed data.

4. References

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