

# Performing Intelligent Power Distribution in a $4 \times 4$ Silicon Photonic Switch Fabric

Christine P. Chen<sup>1\*</sup>, Xiaoliang Zhu<sup>1</sup>, Yang Liu<sup>2</sup>, Qi Li<sup>1</sup>, Johnnie Chan<sup>1</sup>, Tom Baehr-Jones<sup>2</sup>, Michael Hochberg<sup>2</sup>, and Keren Bergman<sup>1</sup>

<sup>1</sup>Dept. of Electrical Engineering, Columbia University, NYC, NY, 10027, <sup>2</sup>Coriant Advanced Technology Group, NYC, NY, 10011

\*Author's email: christinechen@ee.columbia.edu

**Abstract**—A dynamically-programmable optical-power distribution scheme is proposed for increased reliability and energy efficiency in systems. Precise power allocation and intelligent switch control with 40 Gb/s error-free operation is realized on the  $4 \times 4$  multi-stage switch fabric.

## I. INTRODUCTION

The capability to perform high-radix switching will play an integral part in high-speed optical networks envisioned for future datacenter applications and on-chip optical interconnects. Microelectromechanical systems (MEMS), microring resonator based switches [1], and Mach-Zehnder interferometers (MZI) [2] have achieved varying degrees of high bandwidth and low latency characteristics for high-radix switching. Beyond standard switch operations, an important capability of these switches is multicast for applications like optically connected memory [3], where an  $N \times N$  switch fabric can perform up to 1-to- $N$  multicasting. Current switches set switch states to either the cross or bar levels. This scheme does not account for path or power budget variations and is limited in flexibility. A system that can intelligently and dynamically transfer power during multicast will make the switch fabric more reliable and energy-efficient. Traffic rerouting algorithms [4] and increased laser power is bypassed with power redistribution. To perform intelligent multicasting a few improvements are necessary. As the radix of switch networks scales, the control system complexity likewise increases. To account for fabrication variation, an initialization process is necessary to calibrate each device of a multi-stage switch fabric. We present the initialization method to perform fine tuning for each of our broadband switch components, exploring its use as a variable power splitter. After showing the functionality of variable power splitting within the single MZI component, we adapt our initialization process to a  $4 \times 4$  non-blocking switch fabric. We use a high-speed FPGA to accomplish the multicast control. Two power provisioning schemes for multicasting are performed: *ordinary*, where the power at each MZI in the switch fabric is set to 50:50 for either output ports, and *intelligent*, where the power at the final destination of the switch fabric is equalized among clients. Intelligent multicast can be accomplished by varying the power split ratio at the intermediate MZIs.

## II. SWITCH CHARACTERIZATION FOR PRECISE TUNING

The switch devices (Fig. 1a) used in this paper were made through OpSIS [5]. They exhibit a 20 dB extinction

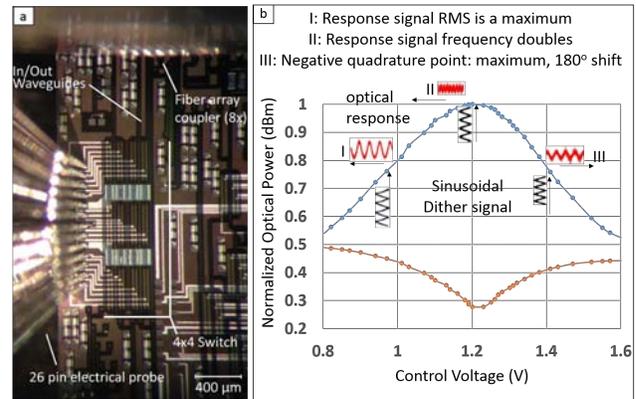


Fig. 1. (a) Microscope image of  $4 \times 4$  (center) switch fabric and (b) dithering technique on  $2 \times 2$  element, which makes up  $4 \times 4$  topology, with scope screenshots overlay on switch characteristics of output 1 (blue) and 2 (orange)

ratio across the C-band and ns-rate switching through carrier injection tuning of an integrated PIN diode. The  $2 \times 2$  switch element is finely characterized via a dithering process traditionally used to initialize laser cavities or dynamically stabilize MZIs [6]. A 500 mVpp, 1 kHz dither signal is applied to the driving signal of one arm of the MZI (Fig. 1b). At the quadrature points of the switch, the root mean square (RMS) value of the dither signal is maximal. When the slope of the switch is negative, its RMS value is again maximal, while the phase of the dither inverts. At the inflection points of the switch response, the frequency of the dither signal becomes double that of the original dither signal. By connecting the output of the switch element to an oscilloscope, these signals can be visualized and precise cross, bar, and midway states are characterized for accurate multicasting results.

We perform the initialization process for the  $4 \times 4$  switch fabric (Fig. 2) by sending light into input 3. Other inputs can be used without loss of generality. First, MZIs in the middle stage of the fabric are tuned to maximize power to one of the output MZIs. In our case we send power to MZ5. Then, MZ5 is tuned to one output port. Finally the input MZI in the first stage is biased with the purpose of increasing power at MZ5. Dithering is done on MZ2, 4, and 5 to fine tune the control voltages. This fully characterizes MZIs in one given path. From here we can determine the cross state control voltages as well as the voltages necessary for arbitrary power split ratios.

With the fabric thus characterized, ordinary vs. intelligent

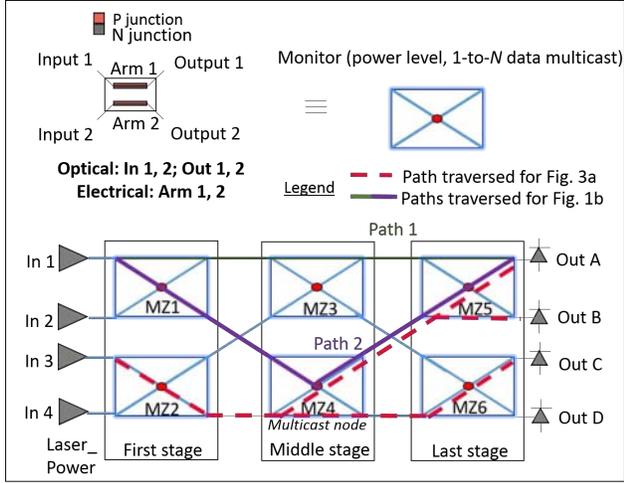


Fig. 2. Cartoon of MZI switch element, embedded in  $4 \times 4$  topology, where multicasting (pink, dotted) is performed, with energy savings looked at on the instance of path 1 (green) and 2 (purple) for system motivation in Sec. IV

switching is performed. Dynamic power allocation is done by programming the fabric to do 1-to-3 multicast at different multicast nodes, with the goal of adjusting the nodes output ratio from 50:50 to 33:66 (Fig. 2).

### III. DATA MULTICASTING FOR INTEGRATED SWITCH FABRIC

Data is modulated at 40 Gb/s onto a 1550-nm CW-laser source (Fig. 3a). A pulse pattern generator (PPG) serves as modulator input, which puts out  $2^{15}-1$  pseudo-random bit sequence (PRBS). The signal is amplified before it is launched on-chip through a fiber array grating coupler. The Xilinx FPGA is used to instantaneously program the switch fabric to values attained through the initialization process, which go through digital to analog converters (DACs). With the control system in place, different multicast operations can easily be obtained. Signals are recovered and amplified before power is varied and received with a high-speed photodetector (PD) for bit error rate (BER) tests (Fig. 3c) with the BER tester (BERT). Eye diagrams are garnered with the digital communication analyzer (DCA) (Fig. 3b). Back-to-Back (B2B) curves are attained by inserting a Variable Optical Attenuator (VOA) tuned to the chips insertion loss.

### IV. DISCUSSION

Fig. 3c shows that the switch can be used to vary different power ratios to different ports when needed, improving the power penalty. With intelligent multicasting, we are able to take the power requirement of each path into account, maximizing energy efficiency in a system. The method for energy savings can be described in the example shown in Fig. 2 where Path 1 has enough power to recover the data, but Path 2 does not. Rather than driving the laser to produce higher optical power, and expending more energy, power is instead reallocated from Path 2 to Path 1. The system then saves on both differential laser driving power and efficiently utilizes the reallocated power. As future datacenters distribute

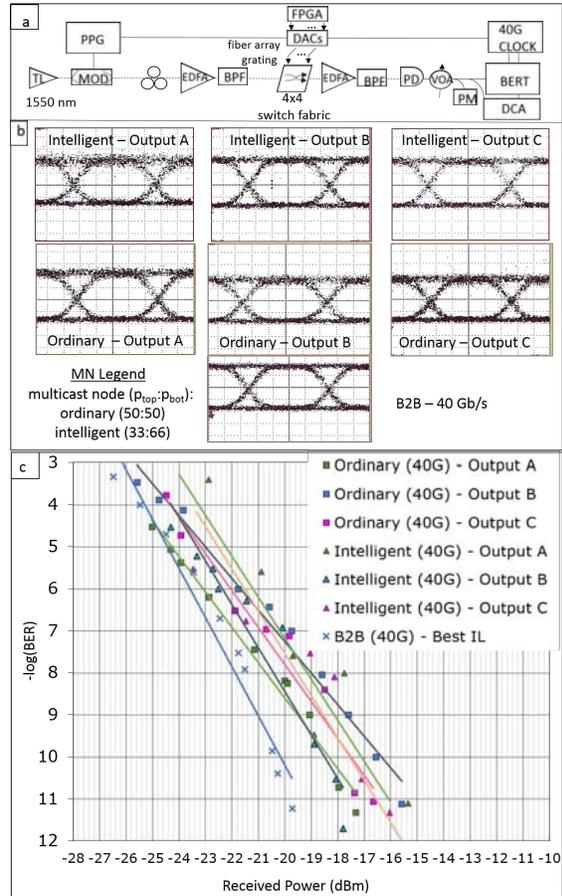


Fig. 3. (a) Experimental setup, (b) eye diagrams, and (c) corresponding BER measurements of 40 Gb/s error-free intelligent multicasting across  $4 \times 4$  fabric

variable loads of data throughout the system, higher bit-rate per energy factors will be needed. With the capability to dynamically reallocate power in a system by an integrated switch, datacenters can move performance towards greater energy efficiency via an intelligent distribution scheme.

### ACKNOWLEDGMENT

We gratefully acknowledge generous support from Intel/SRC Ph.D Fellowship, Columbia IGERT under NSF grant DGE-1069420, and Gernot Pomrenke of AFOSR for funding OpSIS via PECASE award (FA9550-13-0027) and (FA9550-10-1-0439). Thanks also to Noam Ophir for discussions, and Ying Li for wire-bonding.

### REFERENCES

- [1] M. Yang, et al. Non-blocking  $4 \times 4$  Electro-Optic Silicon Switch for On-Chip Photonic Networks, *Optics Express* 19, 47-54 (2011).
- [2] B. G. Lee, et al. High-Performance Modulators and Switches for Silicon Photonic Networks-on-Chip. *Top. in Quant. El.* 16:2 (2010).
- [3] T. Shirashi, et al. Scalability of Silicon Photonic Enabled Optically Connected Memory, *Optical Interconnect* (2014).
- [4] W. Yao, et al. Rerouting schemes for dynamic traffic grooming in optical WDM mesh networks. *GTC, IEEE Comm. Soc.* (2004).
- [5] *Optoelectronic Systems Integration in Silicon*. <http://opsisfoundry.org/> Oct. 2014.
- [6] Salvestrini, J. P., et al. Analysis and Control of the DC Drift in LiNbO<sub>3</sub>-Based Mach-Zehnder Modulators, *JLT*, 29:10 (2010).
- [7] Rawaswami, R., et al. *Optical Networks*, Elsevier, (2010).