Application of a Digital Test Core to a Test Bed for Bit-Parallel Optoelectronic Communications

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Abstract

A programmable FPGA-based digital logic circuit is enhanced with high-speed emitter-couple logic and optoelectronics laser drivers and receivers to create a testbed for evaluating methods of transferring parallel data words in sub-nanosecond bursts. The end application requires the transfer of entire address/data buss information within a single cycle of the computer processor, which is running at several gigahertz. In this paper, the programmable logic core is used to form a low-cost, yet very precise and flexible instrument for emulating the buss activity, converting the data to bit-parallel format, transmitting optically, and capturing the received data. The testbed has been built to demonstrate complete end-to-end operation of a 4-bit parallel slice of the communication channel. Bit periods shorter than 300ps and timing precision of about 20ps is demonstrated.

1. Introduction

Most communication between computers today uses various serial bit stream methods. These allow the use of relatively inexpensive transmission media (such as coaxial cables, twisted-pairs, optical fibers, or wireless RF carrier) to carry the data. Furthermore, since each communication "channel" is made up of just a single physical element, switching and routing of these channels can be accomplished using simple elements distributed throughout the network.

However, the serial communications approach has some drawbacks. Notably, it does not match well with the parallel nature of the data at both the source and destination. Therefore, serial communications relies on parallel-to-serial conversion at the source, and serial-to-parallel conversion at the destination. These conversion processes introduce significant latency (added delay), and may limit the aggregate transfer rate.

To overcome these limitations, yet retain much of the benefits of serial communication methods, a "bit-parallel" approach is under development. The basic idea is to retain the data in its parallel form (as it naturally occurs within the computer systems), convert each bit to a light pulse with a unique wavelength, and combine all the bits into a single optical fiber for transmission across the network. This approach exploits the ability of optical systems to carry multiple signals in parallel without interference within a single physical "channel." In this way, the parallel-to-serial and serial-to-parallel conversions are avoided, and latency is reduced. This method is under investigation as a collaborative effort between Georgia Tech and Columbia University [1,2].

To develop a testbed that would allow characterization, evaluation, and comparison of various methods for bit-parallel communication, a very flexible and in some ways highly specialized set of instrumentation is required. To accurately reproduce (emulate) the buss activity within high-performance computer systems, the test instruments must be able to deal with multiple gigahertz data rates (per channel) and to maintain timing accuracy in the picosecond range. Furthermore, since the end application will require hundreds of simultaneous signals, the instrumentation must be inexpensive. Also, we need to have a wide variation in functionality in order to support testing of the various alternative bit-parallel schemes.

Even with the advanced state of today's automated test equipment (ATE), the needs of this project are difficult to satisfy. This is highlighted by the cost vs. performance of available ATE. The highest performance ATE available today barely meets the needs of current devices, supporting data rates of only 3.2 Gbps. But these testers come at a price of several thousand US dollars per channel, so a 1,000 channel ATE costs several million dollars. Projected prices of ATE systems in the future extend to the $50 million range by 2010 [3]. Additionally, these systems are not expected to be scalable to handle higher-performance devices [4].

In previous papers, the idea of a Digital Test Core (DTC) for testing was introduced [1,2]. A field-programmable gate array (FPGA) is used as both the pin electronics and the interface the test computer. Together with the high speed multiplexing techniques [5], data rates can be increased well into the gigahertz range without relying upon expensive ATE hardware. By extending the support logic to encompass a broad range of functions in a standalone digital test core, test instrumentation cost can be minimized while improving functionality and performance.

In section 2, the concept of the Digital Test Core is reviewed. In section 3, the opto-electronic test bed is presented and performance results are given in section 4. Section 5 concludes by describing the current effort to extend the maximum data rate to 10 Gbps. This includes some preliminary measurements at 4.4 Gbps.

2. Digital Test Core Concept

The digital test core is a reusable, reconfigurable circuit that can be incorporated into various testing scenarios to enhance current test capabilities or to employ new test functions. The DTC includes programmable logic to produce test stimuli and capture output responses through programmable I/Os. Also a provision is made for a large (8Mb) test vector memory. When coupled with additional logic to provide multi-gigahertz speeds and a Universal Serial Bus (USB) bridge to a controlling computer, a miniature tester is created to interface to the device under test.

A block diagram for the digital test core is shown in **Figure 1**. The programmable chip at the center of the digital test core is a Xilinx Virtex-E series field programmable gate array (FPGA). A highlight of the Virtex series is its configurable I/Os that can interface to a wide range of different logic types including low-voltage

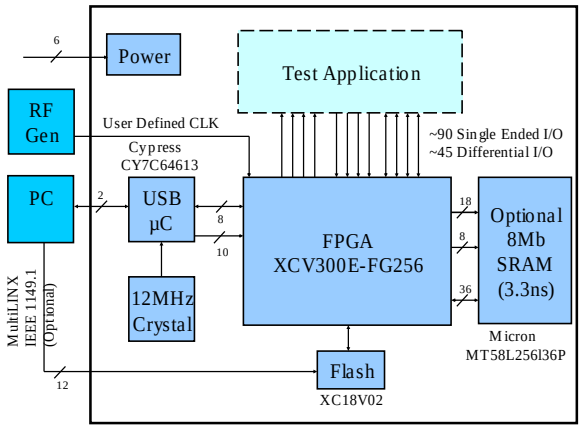

Figure 1. Digital Test Core Block Diagram.

differential PECL. In current designs, the specific chip used is an XCV300E in a 256-pin fine-pitch ball grid array package. The programmable nature of the chip allows test engineers to update and customize tests for future technologies. A computer is needed to provide test data and analyze results, but the critical testing logic is contained within the miniature tester. A Cypress microcontroller (Cypress CY7C64603) is used to process the USB signals and provide the data to and from the Xilinx FPGA. Current versions of the DTC use the USB 1.1 standard which operates at 12Mbps. Future versions of the DTC will use the USB 2.0 standard which operates at a rate of 480 Mbps.

The differential I/Os of the Virtex FPGA were verified to operate at speeds up to 622Mbps as specified by the manufacturer. Newer Virtex series FPGAs have general I/O speeds up to 840Mbps with a few specialized channels operating in the multiple gigabit-per-second range. While these speeds are high enough to compete with currently available ATE, higher speeds and tighter timing accuracy are necessary for some devices.

Current versions of the DTC [1,2] are coupled with external high-speed PECL logic, which times and formats the signals, distributes the clocks, and captures/ preprocesses incoming data. The PECL logic enables operation at higher speeds (~5.0Gbps). Future versions will include SiGe devices to performs similar functions, but operate at much higher-speeds (~10Gbps).

The overall cost of the system depends on the number of channels needed and the test functions required for a specific application. Because the components of the digital test core are all off-the-shelf parts, the cost is orders of magnitudes smaller when compared with multi-million dollar ATE. The DTC may also replace standalone test equipment such as bit-error rate testers, pattern generators, and jitter measurement devices. While most of these standalone devices only provide a few channels, the DTC can provide hundreds, replacing many of these devices in a small package.

The DTC was originally developed for ATE support. It has since evolved so it is now ideally suited for standalone and embedded testing. Two configurations are shown in the next sections.

3. Opto-electronic Pattern Generator/Sampler

Optical testing is considerably more costly due to higher precision and operating frequencies. Traditionally, pattern generators produce signals to the transmitter, which performs the electrical to optical conversion. After the optical transmission, the receivers translate the signal back to bit-error rate testers. This application can benefit greatly from use of the digital test core by replacing costly ATE.

The specific purpose of this research is to develop a test bed for evaluating optical communication within a supercomputer infrastructure. In this application, a four-bit parallel output data is transmitted through coaxial connections to four different wavelength lasers, optically combined through wave-division multiplexing, and then transmitted over a single optical fiber. Incoming data from the fiber is demultiplexed to four-bit parallel electrical pulses, sampled by the PECL circuits, and transmitted to the DTC. A logic block diagram is shown in **Figure 2**. The optical component can also be removed, and the circuit can be used in a loop-back configuration, or as an electronic-only multi-gigahertz tester.

Four-bit words are transmitted during each clock cycle along with a “presence” bit that signals that the data is valid. A trigger bit is also included for output to an oscilloscope for characterization of the board. Four digitally-programmable delay PECL chips set variable pulse widths and delays. The delay range is 10ns with a resolution of 10ps. The four-bit data words are synchronized, while the presence bit is offset to signal when the data is valid.

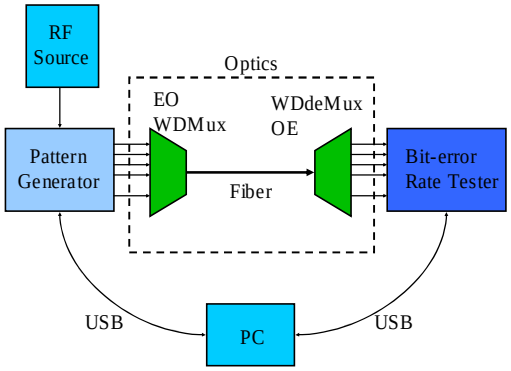

Figure 2. Opto-electronic interface overview.

A high-speed clock is derived directly from the presence bit to capture the received data. The receiver channels are designed to operate either independently or in synchronous operation with the transmitter. The data is captured using a PECL register and returned to the DTC. The DTC can perform simple analysis on the data and then transmit the raw data back to the computer for further analysis. The block diagram for this circuit is shown in **Figure 3**.

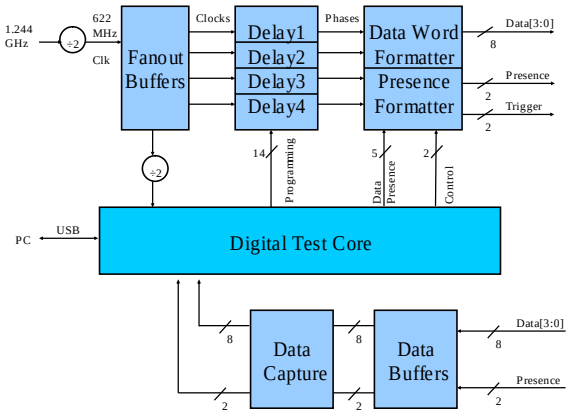

Figure 3. Opto-electronic Tx/Rx Block Diagram.

This opto-electronic transmitter and receiver is shown in **Figure 4**. The DTC is used without the optional SRAM since the on-chip memory in the Virtex FPGA is sufficient for this application. Separate power connections are included to isolate the relatively-noisy CMOS and the high-speed PECL logic. A socket for a PROM is also implemented for automatic programming of the FPGA upon board power-up.

The internal programming of the FPGA is designed to operate in different modes as needed by the user. In one of the modes, a series of four-bit words is entered in the computer and transmitted to DTC. Once the DTC has received the full sequence of test vectors, they are transmitted through the optics at-speed and then received to be stored on the chip. The data is then returned to the user for analysis. In another mode, the DTC transmits a free-running pseudo-random sequence of 4-bit words, and compares them with the returned values. It then stores statistical data, such as number of errors over a given number of cycles. This data is then transmitted back to the user through the USB connection to the PC.

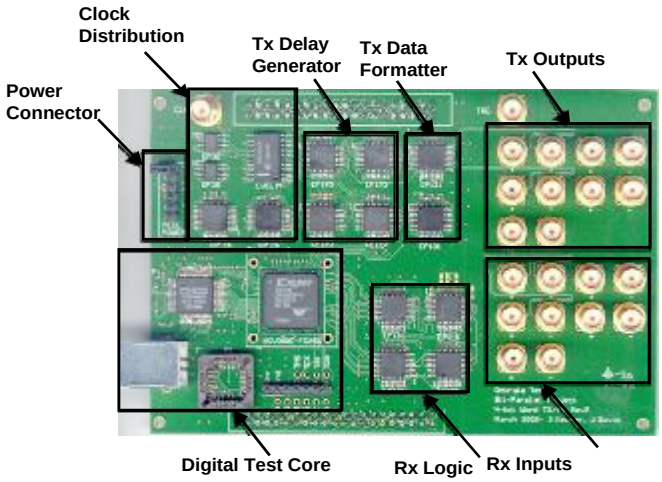

Figure 4. Multi-gigahertz Tx/Rx Photograph [2].

4. Bit-Parallel Communication Test Results

After construction of the miniature tester, an oscilloscope is used to measure the outputs of the four channels as shown in **Figure 5**. This sequence of words (1101,1011) is transmitted in the default return-to-zero fashion. The maximum pulse width of a high logic signal is half of the clock frequency. All four signals are source synchronous on board. Steps must be taken to maintain this off board, such as using matched length cables, since only one set of timing information is provided for all channels. One goal of the wave-division multiplexing scheme is to maintain this source synchronous behavior when returning the data to the DTC.

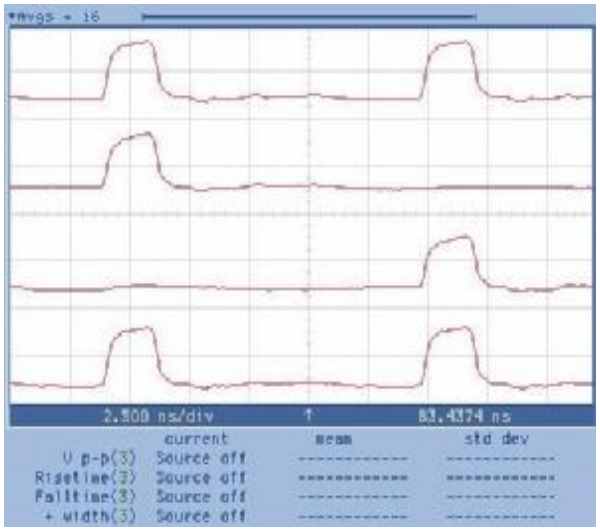

Figure 5. Opto-electronic Transmitter – Two Four-bit-wide Data Words

Even though the maximum data rate of the Virtex chips is 622Mbps, the pulse widths can be shortened by the PECL chips because of their faster rise and fall times. The measured rise and fall times are 150-200ps, which resulted in a minimum pulse width of about 300ps. This proves the data rate of the PECL chips can exceed 3 Gbps per channel. This minimum pulse width is shown in **Figure 6**.

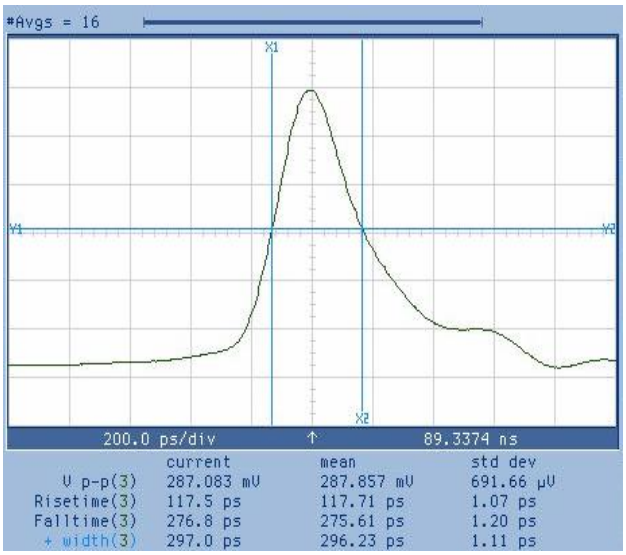

Figure 6. Opto-electronic Transmitter - Minimum Pulse Width (<300ps)

Equally important as short pulse width of the outputs is accurate edge placement. The more precisely the data outputs are placed relative to the presence output, the faster the circuit can operate. If the presence bit operates as a clock to a flip-flop, the setup-and-hold time is minimized with well-timed clock placement. The delay circuits on the board have a resolution of 10ps per step. This means pulse width can be measured with a resolution of 10ps. However, other factors such as jitter can affect the accuracy of the signals. **Figure 7** shows the rising edge of the data output being changed in 20ps increments.

The minimum step size of 10ps achieved by the delay chips. The delay chips are programmed with a 10-bit number, providing a 10ns range. Each of the bits has a certain delay associated with it (10ps, 20ps, 40ps, 80ps, 160ps, etc.), and they add to obtain timing offsets within that range. However, each bit has a certain percent error associated with it. Even with a 1% error of each bit, the impact can be significant. The most significant bit has an offset of 5.12ns, 1% of which is 51ps. These offset errors can contribute to timing inaccuracy and create a non-linearity in the delay programming.

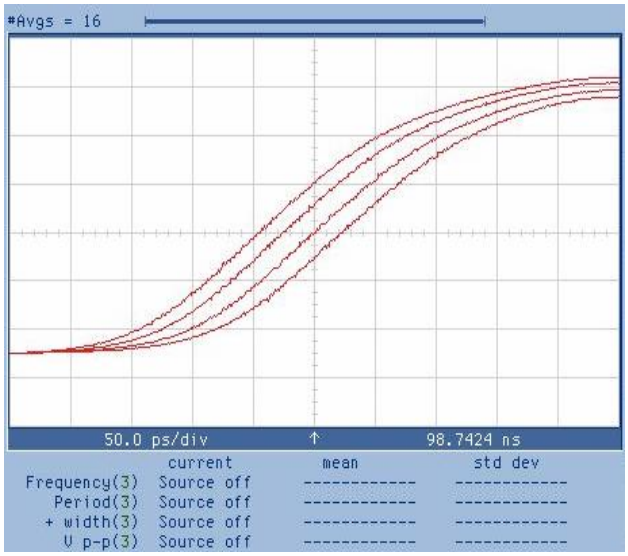

Figure 7. Opto-electronic Transmitter - 20ps Edge Placement Resolution

With edge rates of 150ps, error of even 1% is too high. However, the circuit is designed so that it can be calibrated to still obtain accurate delays (within 10ps). This is accomplished first by measuring the error on each bit of the delay chip. As long as the delays are linear over the whole range, the cumulative error can be computed for every delay value by simply adding the measured delay of each relevant bit. The calibrated delay timing is programmed into the software to automatically set the true delay by searching for the closest matching offset. For example, if the delay is desired to be 150ps, without calibration the actual value is 179ps in one case. By calibrating the circuit, the software programs the value to 120ps, thereby producing an actual delay of 148ps (close to the desired valued of 150ps).

Even with the accuracy of the relative timing, the consistency of the signal is limited by the jitter. From the design of the application, the main contribution of jitter comes from the input clock source. The peak-to-peak jitter is less than 42ps, and the RMS jitter is roughly 6ps, which is less than the timing precision of the DTC (10ps). The statistics are shown in **Figure 8**. If the jitter was higher, the signal edges couldn't be reliably placed within a 10ps resolution. However, when greater precision in the timing is needed (with faster throughput), the jitter must improve as well. Currently the jitter is limited by the RF clock source, so better equipment will be needed for future devices.

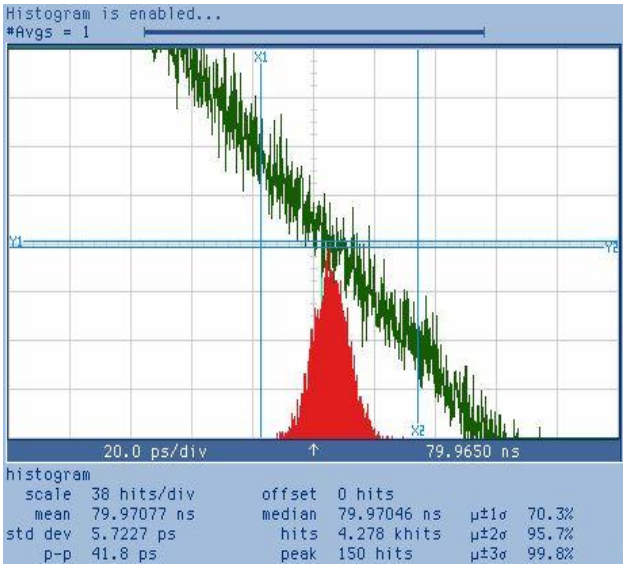

Figure 8. Opto-electronic Transmitter – Jitter Measurements

Once the timing information has been calibrated and programmed, the data is transmitted through the word formatters to the optical transceivers. The optical signal should track the electrical signals exactly in regards to timing. Due to optical requirements, an edge transition must occur within a maximum time interval to maintain signal integrity. Currently, this requirement is ensured by programming the test pattern to include transitions within that interval due to the full manual control of the data stream. Further development of software will provide warning in the event this time interval is exceeded. The electrical to optical conversion is shown in **Figure 9**.

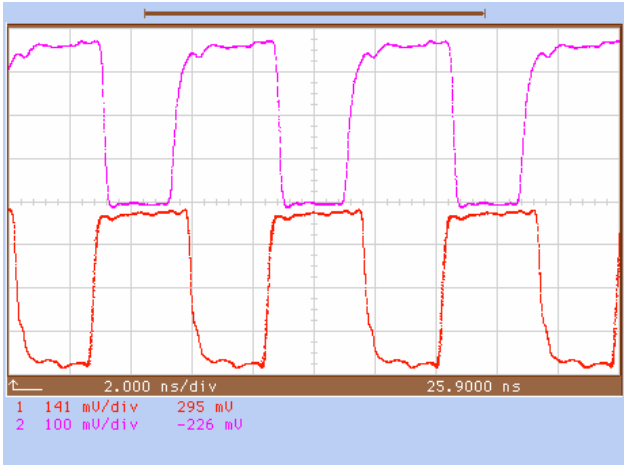

Figure 9. Electrical/Optical Conversion

Some issues remain, such as transmission line effects from connectors, cabling, and oscilloscope probes as can be seen in the Figure 6. With four data channels and a presence channel, all operating differentially, a total of 20 cables are used for the transmitter and receiver. These cables are used to connect the optical and electrical subsystems, since each was being developed by separate research teams. The next generation of this project will be integrated into a single board including all of the electrical and optical components. This will not only simplify the physical aspect of connecting the two systems, but also minimize transmission line effects.

5. Current and Future Work – Extension to 10 Gbps

The next generation of the optoelectronic tester is currently in the design stage. It will operate up to 10Gbps using new SiGe parts. As previously stated, all components will be integrated into one circuit board. The final goal of this project is to reach 128 digital channels combined using wavelength-division multiplexing into one fiber producing an aggregate data rate of 1.28 Terabits-per-second over one optical channel. Since the DTC is designed to easily scale with regards to channel count, this is feasible.

The high-speed timing signals needed for the test have been proven in the previous section to be easily provided by the DTC. In order to increase the data rate, a slightly different approach is used. Many low-speeds signals (622Mbps) are serialized into two half-speed signals each at ~2.5Gbps. These two signals are precisely offset in time and input to a PECL XOR gate producing a high-speed signal at ~5.0Gbps. The returning data is captured and stored in the DTC. The block diagram is shown in **Figure 10**.

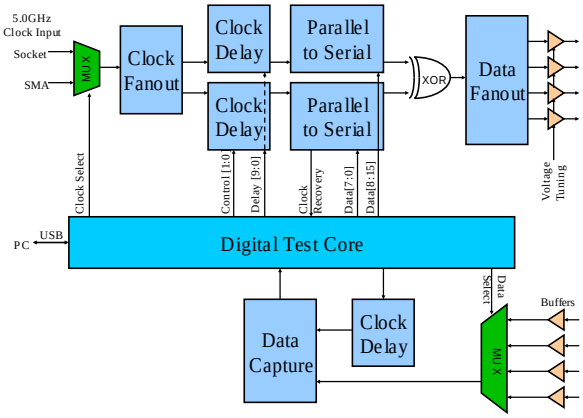

Figure 10. Nano-scale wafer-prober - Block Diagram

The prototype circuit has been partially constructed. The clock signal is input through the SMA connector, or through a multi-pin connector. All test signals are also transmitted through the multi-pin connectors to a motherboard that will have the capability of mounting multiple DTCs. The USB and power are routed through the connectors as well to minimize the cabling when attached to the motherboard, but can also be directly connected to the DTC during development. The clock distribution, timing generation, data multiplexing, and I/O

buffering is handled in the support logic chips surrounding the DTC. The prototype board supports four high-speed differential I/Os.

In preliminary testing, one of the half-speed (~2.5Gbps) signals in the prototype board was measured. The input clock is set to 2.2GHz, and a 1010 pattern is configured by the digital test core. This rate is limited as a result of layout errors in the clock distribution, which are being corrected in a newer version. The high-speed signal is a direct XOR of the two half-speed signals, and with precise timing programming, data rates upwards of 5.0Gbps are expected.

The two half-speed signals and the full-speed signal are shown in **Figure 11**, operating a 4.4Gbps. The bottom two signals (B,C) are the half-speed signals which are sent directly into an XOR gate, producing signal A. The half-speed signals are offset by half a clock period so the high-speed signal have a bit every transition of the clock. Signal C is synchronized with the rising edge of the clock (t1), and signal B is synchronized with the falling edge of the clock (t2). Any bit sequence can be produced with this method, but the two half-speed signals must be properly encoded. The equation for this is described in detail in [6]. The high-speed signal (A) is twice the data rate of the clock. In this situation, the clock is 2.2GHz, and the data rate produced is 4.4Gbps. The circuit is not operating optimally in this preliminary graph as can be seen by the reduced amplitude swing.

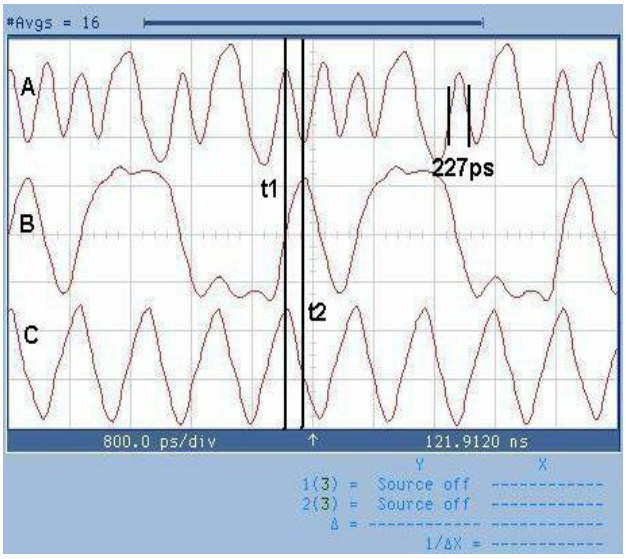

Figure 11. Demonstration of 4.4Gbps Output (A)

Since the DTC is easily scalable, multiple I/Os can be produced using similar techniques. The highest pin density of current programmable logic devices upwards of a thousand of I/Os, each operating at 622Mbps. With the serializing/multiplexing techniques previously described, this can amount to hundreds of multi-gigabit I/Os per DTC. If more I/Os are needed, then multiple instances of the DTC can be used.

As newer technologies develop, such as SiGe, data rates can exceed 10Gbps using similar techniques. With projected rise and fall times of 40ps, coupled with edge placement resolution of less than 10ps, the DTC can be easily upgraded to test the next generation circuits.

5. Conclusions

In this paper we have presented validation of the digital test core as a standalone and embedded tester. The DTC provides a robust interface in multiple testing applications, ranging from a standalone opto-electronic test bed [1] to an embedded wafer-level prober providing an interface to BIST structures in the IC [2]. The DTC also provides programmable precision timing references for at-speed test and characterization of wafer-level packaged ICs. The overall effect of the DTC combines the basic features of ATE, without the high cost; and the test simplification of BIST, but without the complexity of silicon integration.

Acknowledgments

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