Low-Penalty Transmission of High-Speed Data through a Cascade of Silicon Microring Resonator Drop Ports

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Abstract *We demonstrate the propagation of 10-Gb/s optical data through a cascade of microring filter drop ports. The power penalty is measured through two and four resonator hops and compared with simulated values.*

Introduction

Multiple components required for the implementation of ultra-dense high-functionality photonic integrated circuits (PICs) have been recently demonstrated from a collection of passive and active building-block devices in the silicon-on-insulator (SOI) platform [1-3]. A number of these elements rely on the versatility and robustness of microring resonators, which exploit the high index contrast of the material system to implement small-diameter, low-loss travelling-wave devices. These rings can be used for passive filtering applications such as wavelength multiplexers and high-group-delay waveguides [2], as well as leveraged to implement electro-optic and all-optical switches and modulators in active structures [3].

Previous investigations have considered the feasibility of constructing large-scale networks based on microring resonator technology [4-6]. It has been demonstrated, however, that the scalability of such networks can be limited when very high-*Q* resonators are employed, due to the spectral distortion incurred on high-speed signals that propagate through the narrow passbands. We recently reported numerical simulations developed to predict the power penalty associated with this degradation, as well as an experimental validation of the model [7,8]. The effects of narrowband transmission characteristics on signal integrity have been further verified by investigations on slow-light delay applications [9]. Here, we demonstrate penalty-free propagation of a high-speed signal through cascades of two and four microrings, Cascaded devices will be required for networks composed of microring-based switches and filters.

Microring Resonator Cascade

The devices were fabricated on a SOITec SOI substrate with a 3-μm-thick buried oxide (BOX) layer, using electron-beam lithography followed by reactive ion plasma etching. The resulting structure is covered by a 3-μm-thick SiO_2 cladding deposited by plasma-enhanced chemical vapor deposition. The waveguide cross sections are 250 nm × 450 nm (height × width).

The geometry (Fig. 1 inset) is arranged such that two wavelength channels are demultiplexed from the input onto the adjacent waveguide, through two microring resonators (approximately 10 μm in diameter). These channels are then passed to the center waveguide by a second pair of microrings. The longer wavelength exits from output B, while the shorter wavelength is demultiplexed again through another pair of cascaded microrings, and exits from output C. In this structure, we observe cascaded filtering of high-speed data through zero, two, and four microrings by tuning the input wavelength and selecting the desired output.

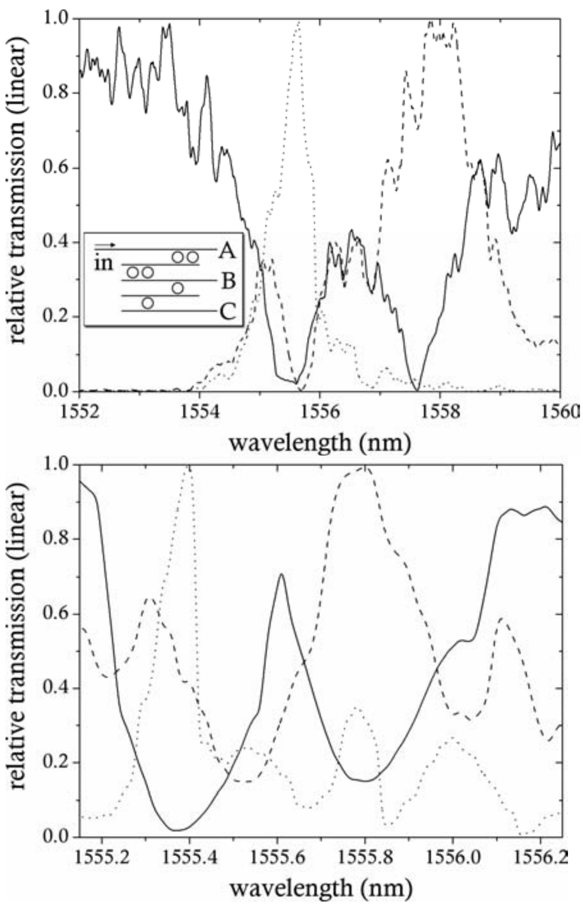

Fig. 1. Transmission spectra of three TM-mode (top) and TE-mode (bottom) outputs: A (solid), B (dashed), and C (dotted), with schematic inset in upper plot.

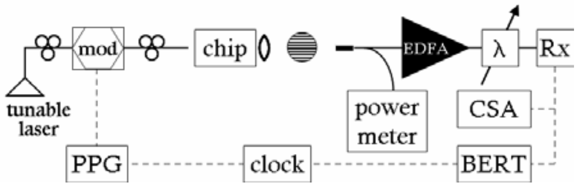

Fig. 2. Diagram of the experimental setup.

Experiment and Results

The setup (Fig. 2) includes a tunable laser externally modulated with a 10-Gb/s non-return-to-zero (NRZ) on-off-keyed (OOK) signal, encoded using a pseudo-random-bit-sequence (PRBS) of length 2^7-1, generated by a pulse pattern generator (PPG). The lightwave is coupled from a tapered fiber to a nanotapered SOI waveguide. After exiting the chip, it is collimated and collected into a fiber; a polarizer is used to select the TM- or TE-like polarization. After propagating through an erbium-doped fiber amplifier (EDFA) and a tunable grating filter (λ), it is received by a high-speed receiver (Rx) with a trans-impedance amplifier/limiting amplifier (TIA/LA) pair. The signal is analyzed with a communications signal analyzer (CSA) and a bit-error-rate (BER) tester (BERT) that is synchronized to the PPG through a 10-GHz clock.

Due to the disparity in confinement between TE and TM modes, the locations and shapes of the resonance spectra for the two modes differ (Fig. 1). In this case, the TM mode resonances experience broader transmission and more overlap from one ring to the next than the TE mode. For this analysis, we have measured power penalties of transmission through both types of modes. Also, because the signals exiting the three outputs experience different on-chip losses, the optical signal-to-noise ratio (OSNR) can be degraded at the input to the EDFA for low-power outputs, causing an increase in overall power penalty. Therefore, a power meter was inserted before the EDFA to evaluate the power during the measurements for each mode.

No power penalty is observed for TM-mode signals propagating through two or four rings (Fig. 3). The simulator predicts a power penalty of less than 0.1 dB for outputs B and C, which is within the experimental error of the measurements. Further, the two-ring TE-mode measurement shows no observable power penalty, and the simulation exhibits a penalty of less than 0.1 dB. The four-ring TE-mode cascade has a 1.5-dB simulated power penalty as a result of its narrower response. The remainder of the 2.7-dB measured power penalty is attributed to OSNR degradation in the EDFA, because the TE power at output C was not equalized with the other ports (as described previously). Additional losses were observed for the TE mode due to the mismatch in its narrower-bandwidth cascaded resonances.

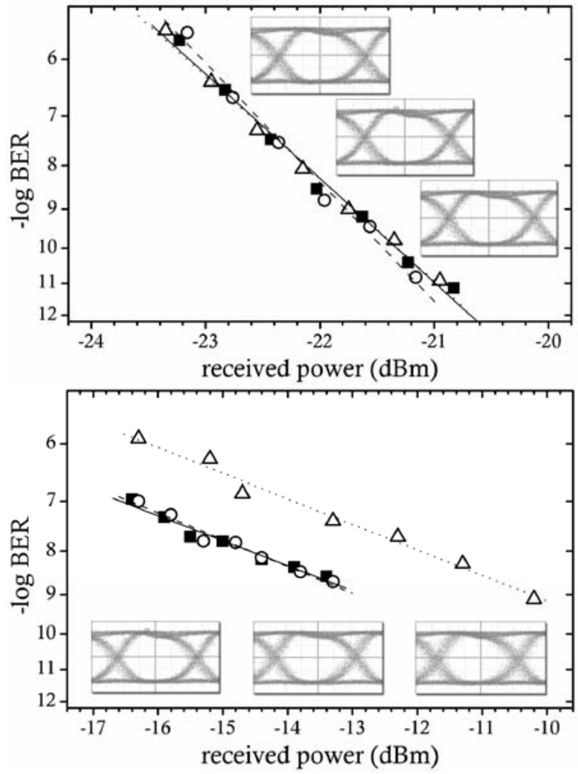

Fig. 3. BER curves for TM (top) and TE (bottom) modes exiting ports A (■), B (○), and C (Δ) with inset eye diagrams from A (left), B (center), and C (right).

Conclusions

We have measured power penalties on a high-speed signal passing through cascaded silicon microrings. Penalty-free operation was observed for all tested signals except the TE cascade through four rings, which experienced a narrower passband (on the order of the signal bandwidth). Using cascaded ring configurations, data routing may be realized in ultra-dense PICs. Future networks may utilize thermal tuning to increase the resonance overlap.

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