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Bit-Error-Rate Characterization of Silicon Four-Wave-Mixing Wavelength Converters at 10 and 40 Gb/s

Benjamin G. Lee[1], Aleksandr Biberman[1], Mark A. Foster[2], Amy C. Turner[3], Michal Lipson[3], Alexander L. Gaeta[2], and Keren Bergman[1]

1: Department of Electrical Engineering, Columbia University, 500 W. 120th Street, New York, NY 10027, USA
2: School of Applied and Engineering Physics, Cornell University, Ithaca, NY 14853, USA
3: School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853, USA
benlee@ee.columbia.edu

Abstract: We present the first bit-error-rate characterization of silicon four-wave-mixing wavelength converters. Power penalties below 0.5 dB are demonstrated over a 20-nm EDFA-limited wavelength range at 10 Gb/s, while 40-Gb/s measurements yield a 2.4-dB power penalty.
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1. Introduction

Optical devices constructed in the silicon platform have recently been shown to deliver exceptional performance in a diverse field of applications ranging from short-haul communications [1] to on-chip global interconnection networks in multi-core microprocessors [2]. The preponderant appeal of silicon photonics stems from its CMOS-process compatibility, which allows low-cost, high-yield fabrication of monolithically integrated optical and electrical circuits. Further advantages are enabled by the large index contrast, which has led to the realization of highly-confined, low-loss waveguides. The ultra-small bending radii now possible have empowered a broad and flexible device design space complemented with immense dispersion tunability. Leveraging this wide dispersion tuning capability, silicon waveguides have become a promising platform for all-optical processing. As a result, wavelength converters [3–5], amplifiers [6], and regenerators [7] based on four-wave mixing (FWM) have already been demonstrated. Such parametric processing capabilities are essential for realizing future transparent optical networks providing access aggregation via ultrafast all-optical data manipulation, which promises to alleviate the bottleneck of current optical-electrical-optical (O/E/O) conversions [8].

Wavelength conversion in silicon waveguides has been demonstrated over more than 150-nm bandwidths using a continuous-wave pump [4]. Moreover, conversion efficiencies have repeatedly been demonstrated in the vicinity of -10 dB [3–5]. Converted optical data streams have been analyzed using time-domain (eye diagrams) and frequency-domain (output spectra) tactics available at the physical layer for both 10-Gb/s [3,4] and 40-Gb/s [5] signals. Quantitative performance metrics, such as bit-error rate (BER) and power penalty, are critical for systems-level characterizations, which analyze the impact of physical-layer distortion on other communications layers, and facilitate the insertion of novel devices into complex networks. In this work, we report the first such system-driven BER and power penalty measurements on wavelength conversion using FWM in silicon waveguides. We obtain error-free conversion (BERs less than 10^{-12}) at bit rates of both 10 and 40 Gb/s. We further demonstrate 10-Gb/s power penalties below 0.5 dB over a 20-nm converted signal wavelength range (1525 to 1545 nm). Although this represents the largest converted signal range over which data-signal conversion in silicon waveguides has been demonstrated, it is limited only by the bandwidths of the erbium-doped fiber amplifiers (EDFAs) used in our testbed, rather than the device bandwidth itself. Finally, a 2.4-dB power penalty is measured for a 40-Gb/s signal converted over 12 nm.

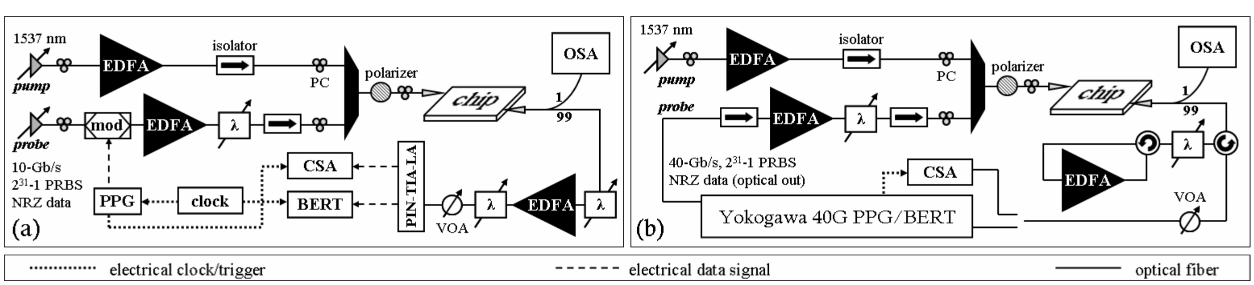

Fig.1. Experimental setup for 10-Gb/s (a) and 40-Gb/s (b) measurements.

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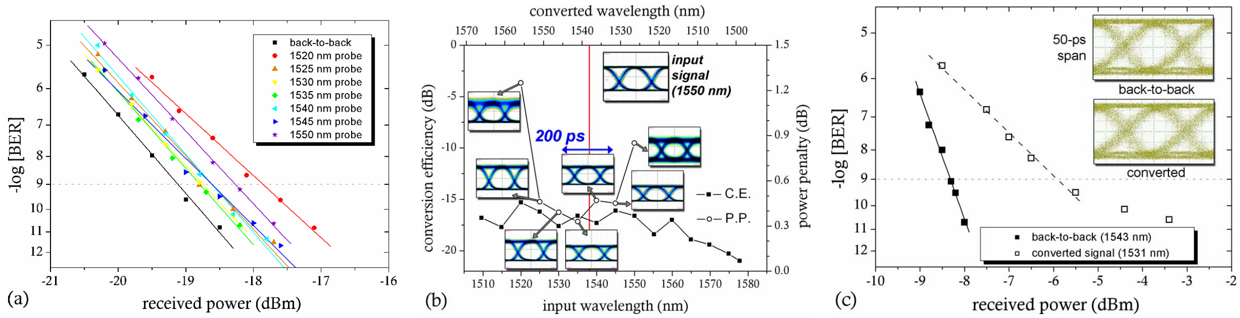

Fig. 2. (a) 10-Gb/s BER curves for converted wavelengths labeled with the input signal wavelength. (b) 10-Gb/s power penalty (○) and conversion efficiency (■) versus wavelength with insets of converted eye diagrams corresponding to each power penalty measurement. The vertical line denotes the location of the pump. (c) 40-Gb/s BER curves with inset eye diagrams before and after wavelength conversion.

2. Experiments and results

The device is a 2-cm-long waveguide with a 300-nm × 450-nm cross section. The fabrication was performed at the Cornell Nanofabrication Facility using electron-beam lithography followed by reactive-ion etching. Each end of the waveguide has an inverse-taper mode-converter for efficient coupling to tapered fibers. The setups for BER measurements (Fig. 1) consist of pump and probe beams coupled together and inserted into the waveguide. Before insertion, the pump and average probe powers are 24 dBm and 15 dBm, respectively. The output power is monitored on an optical spectrum analyzer (OSA), while the signal is received and analyzed using a communications signal analyzer (CSA) and a BER tester (BERT). Further experimental details are depicted in Fig. 1.

Fig. 2a shows BER curves taken on the converted wavelength signal at 10 Gb/s for a variety of input signal wavelengths. The back-to-back curve is taken at the output of the chip on the input probe signal at 1550 nm. The resulting power penalties, obtained at BERs of 10^{-9}, are plotted as a function of both the input signal and converted signal wavelengths (Fig. 2b). A 20-nm wavelength span is shown to exist over which the power penalties remain less than 0.5 dB. The shorter-wavelength edge of the gain spectrum for the input signal booster EDFA causes the rise in power penalty at an input wavelength of 1520 nm (1555 nm converted). The shorter-wavelength edge of the gain spectrum for the pre-amplifying EDFA causes the rise in power penalty at an input wavelength of 1550 nm (1525 nm converted). Therefore, as demonstrated in the conversion efficiency plotted in Fig. 2b, the low-penalty range is limited only by the EDFA gain spectra, rather than the device itself. The pump wavelength (1537 nm), noted in the vertical line in Fig. 2b, was chosen based on the availability of a dense wavelength division multiplexer, but could be further optimized extending the low-penalty conversion range by shifting the pump wavelength to the center of the EDFA gain spectra (about 1545 nm). Finally, 40-Gb/s BER curves are taken (Fig. 2c) using the same pump with an input signal wavelength of 1543 nm (1531 nm converted). The back-to-back curve is taken on the input signal before injection into the waveguide. A 2.4-dB power penalty is obtained at a BER of 10^{-9}. BER measurements with error-free conversion (BERs less than 10^{-12}) are observed with higher received power (see eye diagram insets in Fig. 2c). The noise floor and altered slope of the converted signal's BER curve is attributed to the use of low-quality optical bandpass filters, which are not optimized for 40-Gb/s data.

3. Conclusion

We have characterized a silicon wavelength converter with extensive BER measurements at 10 Gb/s, resulting in marginal power penalties over a 20-nm bandwidth. We have also demonstrated error-free 40-Gb/s wavelength conversion with a 2.4-dB power penalty. These results provide a significant advancement toward the integration of ultrafast all-optical parametric processing devices within large-scale optical networking systems.

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