

Bistable Switching Node for Optical Packet Switched Networks

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Abstract- We demonstrate a 2×2 semiconductor optical amplifier based switch element with robustness to optical routing glitch errors. This improvement is achieved using Schmitt trigger comparators in the routing decision logic.

I. INTRODUCTION

Optical packet switched (OPS) interconnection networks have been suggested as possible solutions for applications requiring high-capacity data routing with low communication latency. Depending on the network size, possible applications range from local area data communication and storage to high-performance computing [1]. In multistage OPS networks, optical packets propagate through a number of cascaded switching nodes proportional to $\log_2(N)$ for an $N \times N$ port network [1]. Consequently, the node routing efficiency directly impacts the latency, throughput and overall scalability of the network. The predominant switching element used in highly scalable OPS networks is the commercially available semiconductor optical amplifiers (SOA). Besides acting as a gate to route packets to their destination, the SOA compensates for optical power losses and has the ability to route wavelength division multiplexed (WDM) optical packets. The simplest internal node can be a 2×2 self-routing switching element containing two SOA devices as used in the data vortex network architecture [2]. In this network topology, the node is transparent to the routed packet payload. Consequently, possible bit errors in the payload data are reversible using data encoding at the source or forward error correction at the destination. However, self-routed networks rely heavily on error-free routing at the internal switching nodes. Hence, any error in processing the routing decision can have dramatic effects on the network performance, i.e. loss of the packet and collisions with other routed packets.

In this paper, we report on a design optimization in SOA-based switching node by incorporating Schmitt trigger comparators within the routing logic. The added bistability feature improves the switching node robustness of the routing decision to glitches occurring in the encoded header signal. The optimized node incorporates an additional improvement recently reported in [3], contributing to higher network data throughput by reducing the guard times within the packet structure. The switching time of the SOA was

improved by 40 % compared to currently available SOA devices, through a hybrid integration of an SOA with its current driver. The two optimizations, robustness to routing glitches and fast switching SOA (DSOA) shown in Fig. 1, are thought to be key features in enabling higher data throughput and network scalability.

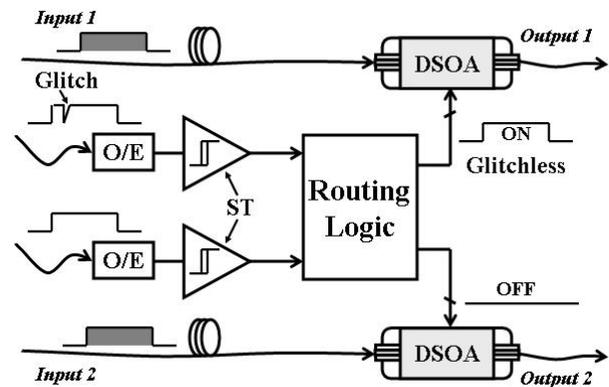


Fig. 1 Schematic of optimization made to a 2×2 switching node for glitchless operation. Schmitt trigger (ST) comparators are prior to the routing logic, following the optical to electrical conversion (O/E) of the control channels. Packet is delayed while processing the routing decision.

II. SWITCHING NODE OPERATION

In the data vortex self-routed network [2], the routing decision is electronically processed at the switching node level from information contained in the packet header field. Header and frame bit information are encoded along specific wavelengths within the multiple wavelength optical packet structure. Their bit value remains constant throughout the duration of the packet. The frame bit indicates the presence of a valid packet and the remaining header bits encode the destination address. At each switching node the frame and one of the header bits are filtered and converted to electrical signals. Routing is accomplished by enabling one of the two SOAs in accordance with the routing decision.

As packets propagate through a cascade of switching nodes, amplified spontaneous emission (ASE) noise accumulates, increasing the optical power in the packet. Additionally, nonlinear effects such as cross-gain modulation between the payload channels can create erratic

changes in the optical [4]. At the node level, optical detectors with high sensitivity convert the encoded routing header and frame of the packet to electrical signals. A complex programmable logic device (CPLD) contains the routing logic derived from the OPS network architecture. The electrical routing decision signal enables one of the two SOA devices of the 2×2 switching node (Fig. 1). The packet is then routed either through the primary or secondary output port. A change in the incident optical power on the optical detectors can change the electrical routing decision signal and consequently affect the state of the SOA devices. This would lead to truncation of the routed packet if the SOA is falsely disabled.

III. GLITCHLESS OPERATION

To mitigate the effect of noise on the optical detectors, Schmitt trigger comparators are added prior to the routing decision [5]. Due to the Schmitt trigger hysteresis, a noisy header signal may have a voltage value below the high threshold value, but the output signal will not go to zero unless it is below the low threshold value. The Schmitt trigger inputs of the CPLD are used with an input hysteresis threshold voltage at 80 % (V_{T+}) of the input high and 20 % (V_{T-}) of input low. When the input is below V_{T-} , the output is low; when the input is above V_{T+} , the output is high; and when the input is between the two thresholds, the output retains its value for a more stable and robust switching node.

The O/E conversion consists of a p-i-n integrated with a transimpedance amplifier (TIA), followed by a limiting amplifier (LA) digitizing the received signal. The conversion is entirely DC-coupled allowing for burst mode reception. A fixed decision threshold value is used in the limiting amplifier. With only one input threshold, the limiting amplifier rapidly switches back and forth from a low to high when a noisy incident signal is near its threshold value. In Fig. 2, we show the output signal of the O/E conversion when a glitch is present in the incident optical signal to the detectors. The Schmitt trigger comparator removes the glitch since the signal change is not large enough. The electrical routing decision signal exhibits no glitch. The SOA is therefore properly enabled without a false switching state that would truncate the packet.

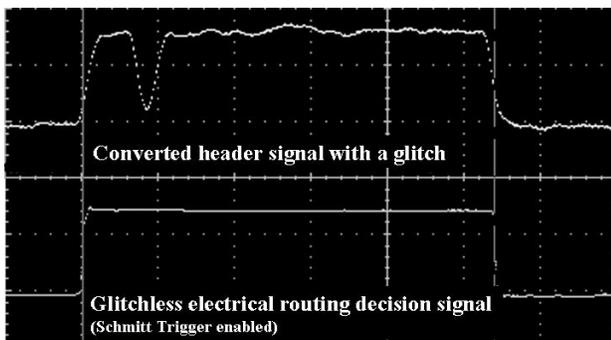


Fig. 2: Electrical header signal with an unwanted glitch (top). Glitchless routing decision signal enabling one of the two DSOA devices (bottom).

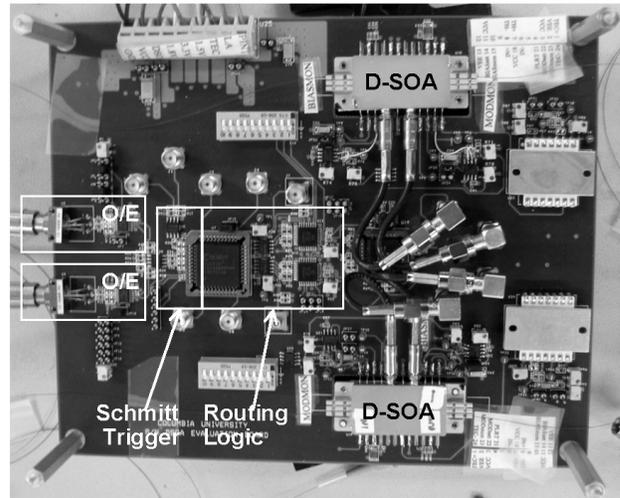


Fig. 3: Implemented switching node with Schmitt trigger comparators.

In Fig. 3, the implementation of the SOA-based 2×2 switching node is shown with the glitchless features and high data throughput DSOA devices. The node is implemented on a FR4 printed circuit board and the Schmitt trigger comparators are integrated within the routing logic.

IV. CONCLUSION

We demonstrated a bistable 2×2 SOA-based switching node designed for OPS networks. The optimized switching node makes use of Schmitt trigger comparators for greater noise immunity and the elimination of fatal packet routing errors. This optimization directly impacts the overall throughput, scalability, and robustness of OPS networks.

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