Hybrid Integration of a Semiconductor Optical Amplifier for High Throughput Optical Packet Switched Interconnection Networks

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ABSTRACT

Higher data throughput in optical packet switched interconnection networks can be achieved by minimizing the guard times through faster transition of the switching element. A hybrid integration of a semiconductor optical amplifier with its current driver is presented, which exhibits over 40 % faster transition time compared to current commercial devices.

Keywords: Optical interconnects, optoelectronics packaging

1. INTRODUCTION

Optical packet switched (OPS) interconnection networks are a promising means of routing high bandwidth optical packets with low communication latency. Depending on the network size, possible applications range from high-performance computing and data communications to storage area networks and high-capacity telecom routers [1]. In typical banyan multistage OPS networks, optical packets propagate through a number of cascaded switching nodes proportional to $\log_2(N)$ for an $N \times N$ port network [1]. Consequently, the node routing efficiency directly impacts the latency, throughput, and overall scalability of the network. One predominant switching element used in highly scalable OPS networks is the commercially available optical semiconductor amplifiers (SOA) due to its broad gain bandwidth, high extinction ratio, and potential for integration with optical and electrical devices. The simplest internal node can be a 2×2 self-routing switching element containing two SOA devices as used in the data vortex network architecture [2]. In this application, the SOA devices are used as switching gates to transparently route individual packets containing multiple WDM channels at high data rates (10 Gb/s or 40 Gb/s). The routing decision is electronically processed at the switching node level, then a current driver enables the SOA to allow the packet to propagate in one path or disables the SOA to block the packet in another path. Besides acting as a gate, the SOA compensates for small optical power losses from the passive optical components of the node structure such as couplers, delay lines and connectors.

In commercial SOAs the parasitic capacitance and inductance of standard butterfly packages limit switching transition times. This paper presents a hybrid integration of a high-speed current driver with an SOA (D-SOA) as a solution towards a faster switch transition time and improved throughput of interconnection networks. A significant 40 % improvement in the transition time is demonstrated from 900 ps for commercial SOA down to 500 ps for the D-SOA.

2. AN SOA-BASED NETWORK TOPOLOGY OVERVIEW

The data vortex is a self-routing deflection network topologically scalable for large (e.g., 10k-port) interconnections and specifically designed for implementation with photonic technologies [2]. Its deflection routing mechanism eliminates the need for internal optical buffering while meeting large-scale interconnection networks' key requirements of low switching latency and high throughput. The system illustrated in Fig. 1 corresponds to a switch fabric supporting 12 input and 12 output ports. As illustrated, packets enter from input nodes at the outermost cylinder and exit from output nodes at the innermost cylinder. Upon entering a node, the packets are routed based on the destination address encoded in the header signal and the deflection signaling from an adjacent node. If the address does not match the user-programmed value, or if the next node is busy, the packet is deflected. If the destination output buffers are busy, the innermost cylinder allows the packet to circulate.

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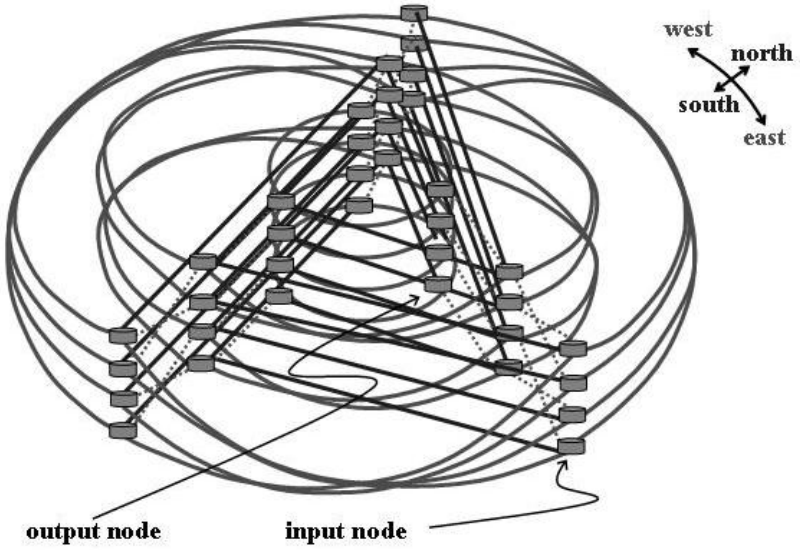

Fig. 1. Data vortex topology corresponding to a 12-port interconnection network that contains 36 switching nodes.

In this time-slotted network architecture, one packet at a time is processed within each node in a particular timeslot. The routing decision is electronically processed at the switching node level from information contained in the packet header field. Header and frame bit information are encoded along specific wavelengths within the multiple wavelength optical packet structure. Their bit value remains constant throughout the duration of the packet. The frame bit indicates the presence of a valid packet and the remaining header bits encode the destination address. An example of a wavelength-parallel packet structure for an OPS network is shown in Fig. 2. The rest of the packet can be used for data payload at higher data rates detected only when the packet reaches its destination. In this packet structure, dead time (3.3 ns) is used to separate each packet. Guard time (1.6 ns) is inserted at both the beginning and the end of the packet. This requirement is necessary because of the finite transition time of the SOA. The slot time is determined by the topology used. In this network, the slot time is 25.7 ns. Small packet length in the order of 10's of nanosecond is favoured to allow packet granularity.

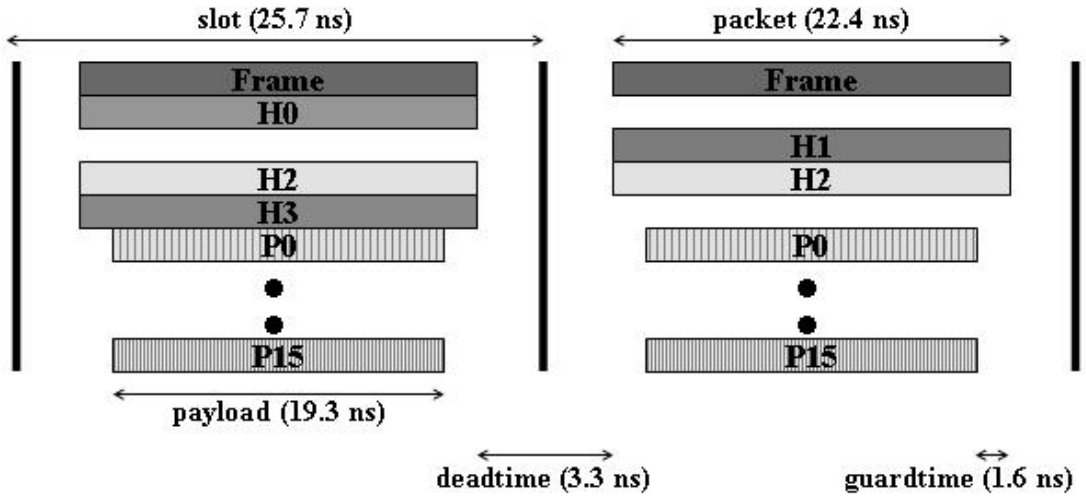

Fig. 2. Packet structure: payload and routing headers encoded on DWDM channels.

The simplest internal node is a 2 × 2 self-routing switching node containing two SOA devices as shown in Fig. 3. At each switching node the frame and one of the header bits are filtered and converted to electrical PECL level signals. The routing decision is electronically processed at the node based on the frame and header information using high-speed positive coupled emitter logic (PECL) gates. Meanwhile, the packet is delayed through fiber. Once the routing decision is processed, a current driver takes the PECL level electrical signal and enables one of the two SOAs. The gain of the SOA is set by the forward current to the SOA. In this node structure, the gain is preset to 6 dB to compensate for the node loss due to the couplers and connectors. The enabled SOA will route the packet through that output port of the node, while the other SOA will absorb and block the packet. The packet is efficiently routed through only one of the two output ports.

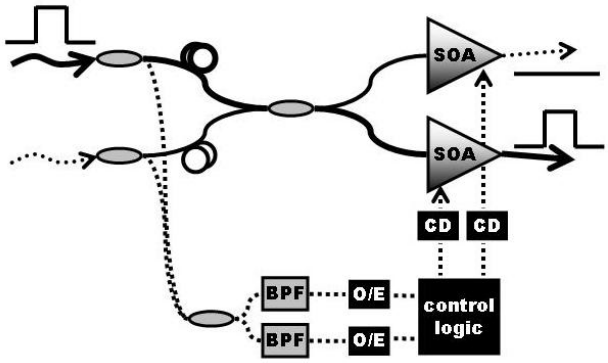

Fig. 3: Switching node configuration of the data vortex network with a single packet being routed through one output port (BPF: optical bandpass filter, O/E: optical-to-electrical conversion, CD: current driver).

3. HYBRID INTEGRATION

Electrical signals with fast edges can be obtained with state-of-the-art logic gates processing the routing decision. However, the optical response is limited by the interface between the current driver and the active region of the SOA. The trace signal from the current driver to the SOA is bandwidth limited affecting the transition time. More significantly, the parasitic inductance of the butterfly package pins and the capacitance load of the active region degrade the optical response of the SOA. Unfortunately, this transient response of the SOA directly maps to the gain affecting the payload data. An RF matching network at the cathode of the active region can help improve the optical response, but this requires tuning at every node which becomes difficult in multistage OPS networks. Consequently, the SOA optical response does not map exactly to the digital routing decision signal and the data at the leading edge of the packet is typically unreliable. Larger guard time can compensate for the loss of data at the beginning of the packet, but at the cost of the overall network throughput. The required guard times arise from this finite switching times and the transient response of the SOA is approximately 0.9 ns with current devices [2], [3].

We developed a solution to reduce the signal distortion as well as the transition time by combining a current driver with the SOA device in a temperature controlled hybrid integration platform. A 10.7 Gb/s current driver (MAX3934) die of 1.30mm × 1.35 mm is bonded to the SOA active region within a modified 28-pin butterfly package (Fig. 4). The current driver accepts standard digital 5-Volt PECL level signal, hence the acronym D-SOA for Digital SOA. The package has two high frequency Sub-SMB input connectors preserving the signal integrity of the differential digital logic signal that enables the D-SOA as the packet is routed through the node. Additionally, the current driver has an integrated compensation network consisting of a series-damping resistor and a shunt RC optimized for 0.4 nH inductance for the bond wire.

Besides acting as a gate, the D-SOA gain compensates for small optical power losses from the passive optical components of the node structure. The current driver can inject up to 100 mA to the SOA which corresponds to a gain of 6 dB. The preset gain of the D-SOA is controlled by the internal current driver and is externally tuned through pin *Vgain*. A small DC current is provided to the D-SOA through pin *Vbmon* maintaining the appropriate carrier density for a faster transition time. Both the gain and the bias are monitored through pin *Vgmon* and *Vbmon*, respectively.

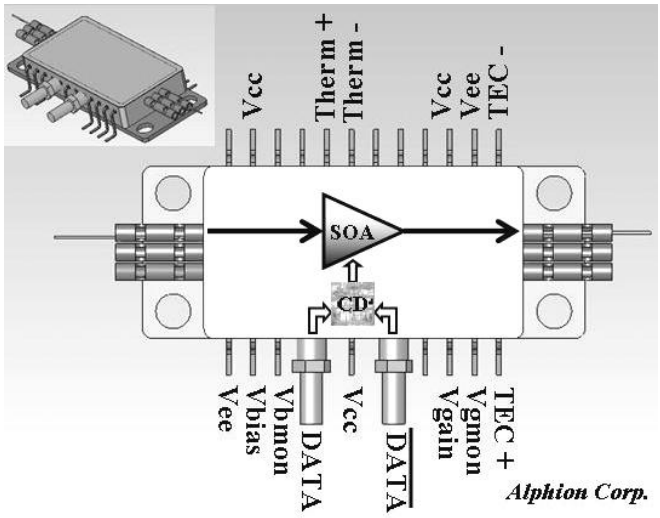

Fig. 4. D-SOA pin-out. Modified 28-pin butterfly package with two sub-SMB connectors (inset).

4. RESULTS

The D-SOA constitutes one of the switching node optimizations implemented on a prototype evaluation board shown in Fig. 5. The D-SOA is enabled by the routing decision signal or by an external high bandwidth signal generator for a more comprehensive characterization. For this work, a fast programmable pattern generator generates the electrical signal corresponding to a processed routing decision that would enable the D-SOA. The bias is set to maintain the carrier density closer to the threshold current without exceeding it to avoid the propagation of noise through the network. External operational amplifiers are used to regulate both the bias and the modulation current by comparing the set value with the monitored values. To characterize the optical responses of the DSOA, a DFB laser emitting at 1553 nm followed by an attenuator to control the input power to the SOA is used. The continuous wave signal input power is set to -13 dBm. The D-SOA has a saturation input power of -2 dBm and operates in the linear regime. The output is amplified and filtered prior to the scope with an 20 GHz optical module.

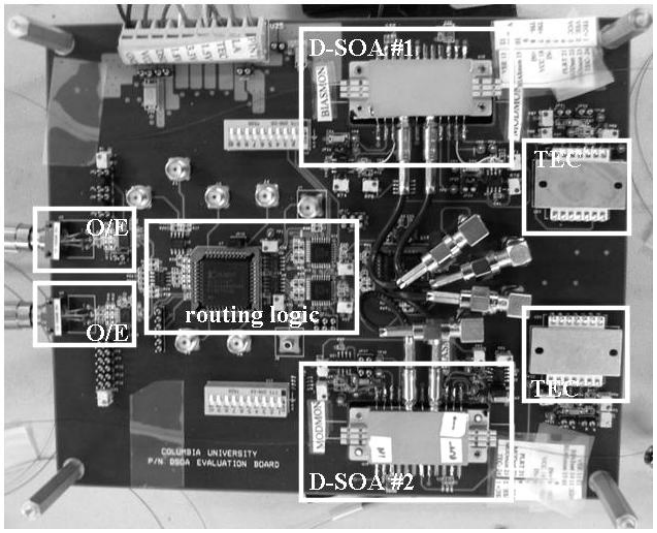

Fig.5. Optimized SOA-based switching node with two temperature-controlled D-SOA devices, optical receiver (O/E) and routing logic.

Characterization results of the D-SOA are compared to commercial SOA devices (Fig. 6). For a WDM channel at 1545 nm, the measured transition time (20%-80%) is 500 ps for the D-SOA compared to 900 ps in a commercial SOA. This corresponds to a 44 % improvement in the switching transition time for a gain set to 6 dB. Additionally, the overall optical response of the D-SOA does not exhibit as much ripple compared to the commercial SOA.

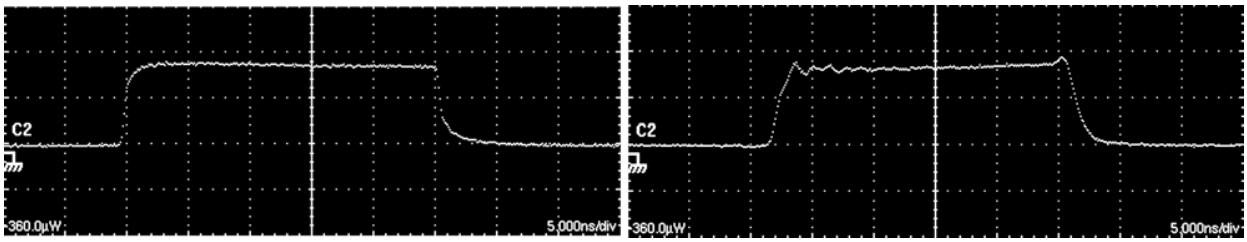

Fig. 6. Optical signal at the output of the D-SOA (left) and of a commercial SOA (right).

5. CONCLUSIONS

Hybrid integration of a semiconductor optical amplifier with a 10.7 Gb/s current driver die in a temperature-controlled 28-pin modified butterfly package shows over 40 % reduction of the switching transition time over a commercial SOA. Additionally, a qualitative improvement in the overall optical response is observed. The faster transition time enables a reduction in the required guard times of optical packets in multistage-switched networks. These results in enhance overall network data throughput as more payload data can be reliably encoded within the same time slot.

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