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WDM Routing with Low Cross-Talk in the Data Vortex Packet Switching Fabric

W. Lu, K. Bergman, *Columbia University, New York, NY;* Q. Yang, *Harvey Mudd College, Claremont, CA, Email: bergman@ee.columbia.edu*.

Routing of 10Gbit/sec optical packets is demonstrated with WDM-encoded header bits. The traffic flow control mechanism uniquely reduces latency and simplifies packet processing. Significantly lower cross-talk is obtained using linear optical amplifier switching gates.

1. Introduction

Photonic packet switching presents a potentially attractive way to alleviate the electronic bottleneck in communication and computing networks. Recently, major advances in optical packet switches exploited the unique advantages of optics employing techniques such as optical-label swapping and all-optical wavelength conversion [1-3]. The commercial success of photonic switching fabrics has been largely limited however by economic as well as by critical technical challenges. Functions that are easily performed electronically such as packet buffering and intelligent control present formidable challenges when done optically, severely limiting the practical scalability of the switch fabric [4]. We have recently proposed and experimentally demonstrated a switching fabric architecture, termed the Data Vortex, that employs synchronous control signaling for packet flow control which greatly simplifies the processing required and eliminates the need for buffers [5,6]. Semiconductor optical amplifiers (SOA) are the preferred technology for the switch elements since they consume low power and offer the potential for multiple device integration. One major drawback of SOAs has been the cross-talk generated between WDM channels, which limited the scope of WDM routing in the Data Vortex.

In this paper, we demonstrate WDM 10Gbit/sec packet routing through two fully functional routing nodes of the Data Vortex. The header bits are encoded in a WDM bit-parallel fashion where every bit occupies a separate wavelength. This arrangement significantly simplifies the routing and reduces the overall latency. For the packets' 10Gbit payloads two additional wavelength channels are used. One of the two nodes is constructed from a Linear Optical Amplifier (LOA) gate [7]. The second node, used for performance comparison, is built from an SOA gate switch. The cross-talk between the WDM payload data channels emerging from the LOA-node is greatly reduced.

2. Data Vortex Architecture

The Data Vortex switch architecture consists of switching elements (i.e. routing nodes) arranged on a collection of concentric cylinders, as shown in Fig. 1. The size of the switch fabric is characterized by the parameters A and H, corresponding to the number of routing nodes lying along the "angle" and "height" dimension respectively. The number of cylinders, C scales as $C=\log_2(H)+1$. Each routing node is labeled by the three parameters (a,c,h). Packets flow from the most outer cylinder to the most inner cylinder unidirectionally. The connection links within the cylinders cross in a binary tree fashion to fix the next most significant bit of the header address before the packet is forwarded to an inner cylinder level. The connections between cylinders simply forward packets maintaining the packet height. A more detailed discussion of the Data Vortex architecture is provided in [8].

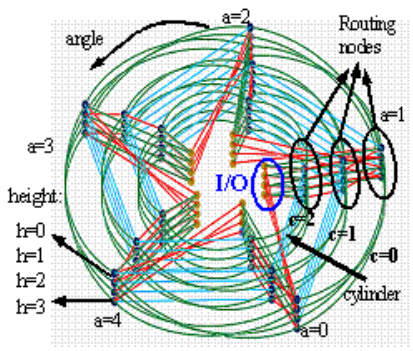

Fig.1 Schematic of the Data Vortex topology with A=5, H=4. The routing nodes are interconnected on C=3 concentric cylinders.

The switching fabric operates in a synchronized manner and each packet moves one angle forward within a clock cycle. As the packets propagate from the outer cylinder towards the inner cylinder, only a single bit of their target height address is decoded within the routing nodes. To further simplify the processing at the nodes and remove the need for buffering, a distributed control signaling is used to ensure that only a single packet enters a node in any given clock cycle. This eliminates the complication of performing packets contention resolution.

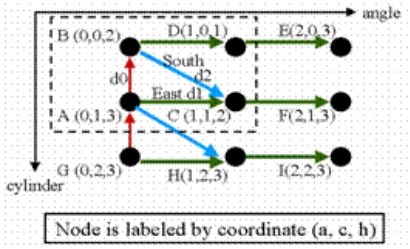

Fig.2 Control signaling between competing nodes.

The control message flow is illustrated in Fig. 2, where as an example, packets at inner cylinder Node A and outer cylinder Node B are both destined for the same output port to Node C. A control signal from A to B is used to deflect the packet in Node B to Node D, since inner Node A always has priority. The deflected packet now at Node D will be in a position to drop "South" toward the inner cylinder after one additional hop. Note that an open (deflection) path, on the same cylinder level, is always available under this priority scheme.

3. Experimental setup

Fig. 3(a) shows the experimental setup. Each packet is constructed with two header channels at λ1=1547.7nm and λ2=1550.9nm for header bits H_1 and H_2 such that (H_2H_1) represents the binary destination address. A framing channel at λ3=1555.6nm is programmed to indicate the presence of a packet in the time slot. Two payload channels at λ4=1545.3nm and λ5=1553.3 nm are encoded with data at 10Gb/sec. Thus, the entire packet is located within the time slot of one header bit, reducing the processing latency. Node B represents an outer cylinder node and is constructed with LOA switching gates. The LOA integrates a vertical cavity surface emitting laser and an amplifier that share the same gain region [7]. The vertical laser linearizes the amplifier and provides a flat gain response that minimizes WDM cross-talk through the LOA. Node A is an inner cylinder node built with SOA switches. At each routing node only one of the header bits is decoded. Thus node A only decodes the H_1-bit of the incoming packet using a 1nm band-pass filter centered at λ1. Similarly node B employs a filter at λ2 to decode the H_2-bit. The traffic control signal for node A is programmed directly from PPG1 for flexibility, while the control for node B is generated from the routing logic circuitry of node A. Packets arriving at node B are delayed with respect to packets at node A. This allows Control_2 to set up. This delay is determined by the decision circuitry delay (1.6ns) and by the connection setup time (3ns). As shown in Fig. 3(b), within each node, a small amount of optical power is tapped off the entire packet, followed by an appropriate filter for the header bit retrieval. The detected header bit and control bit are used in the decision logic, which then outputs the appropriate drive signal for the LOA/SOA switch.

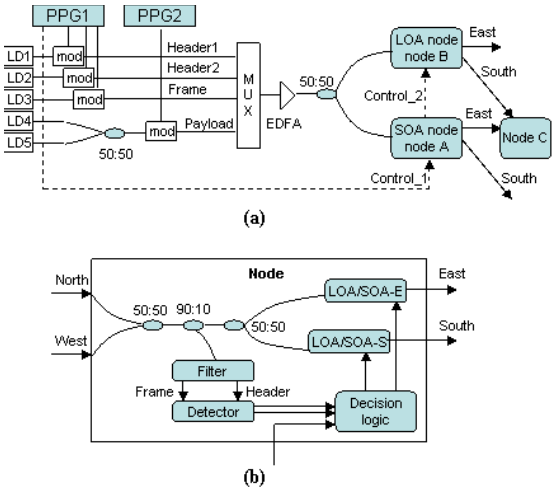

Fig. 3 (a) Two-node WDM routing test-bed schematic. (b) Routing node structure. PPG: pulse pattern generator; LD: laser diode; EDFA: Erbium doped fiber amplifier; LOA: linear optical amplifier; SOA: semiconductor optical amplifier.

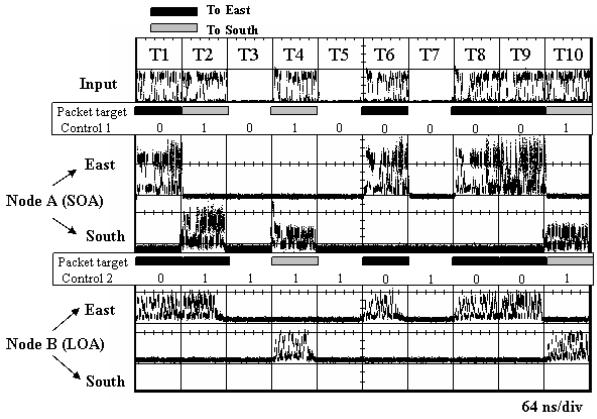

Fig.4 Routing results at node A (SOA) and node B (LOA) from payload channel at λ5=1553.3nm. A similar result is obtained from payload channel at λ4=1545.3nm.

4. Results

To demonstrate the control signaling, we programmed a short sequence of 10 packets, each carrying different routing destinations. The packets are 64ns long, including a 6.4ns guard time at the edge of the packet boundary to allow for the routing transients.

For a specific input sequence INPUT into the inner cylinder node A, shown at the top trace in Fig.4, we randomly set its control sequence to be "01010,00001", where Control_1=0 means "deflect" and Control_1=1 means "do not deflect" the message intended for the packet slot. Combining the packet target of each incoming packet with the control signal yields the routing result to either the East or South ports of the node. The routed packets at the East and South output ports of node A are shown as the middle 2 traces in Fig. 4. As evident from these traces the packets were routed successfully in accordance with the programmed routing logic. As a further confirmation of the correct routing we examine the generated control signal (Control_2) at node B. We expect a "deflect" control message to be triggered whenever node A sends a packet to its East port (node C). Consequently, the expected Control_2 sequence for the experiment shown is "01111,01001." Finally, the routing output through node B is determined by the packet target arriving at B and by the control signal Control_2. The routing results from node B are shown at the last two traces in Fig.4, confirming the correct implementation of the control scheme within the test-bed.

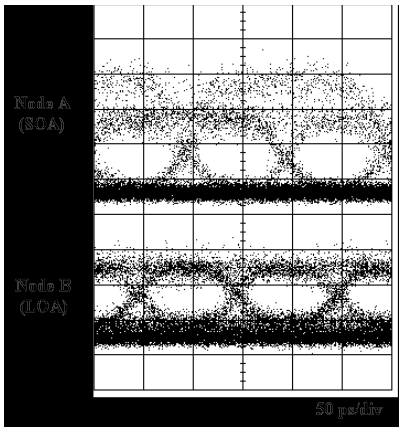

Fig. 5. Eye diagrams at switch output (south) from payload channel at λ5=1553.3nm. Upper trace represents output from node A (SOA gate) and lower trace represents output from node B (LOA gate).

We note in Fig. 4 that for the SOA node A, packets in different time slots have varying power levels. This is due to the fact that the presence (or absence) of signal in the header channels affects the gain of the payload channels. This cross-talk is greatly mitigated at LOA node B, in which the different packets have more uniform power levels. Fig. 5 shows the payload eye diagrams emerging from the SOA node A (top 2 traces) and from the LOA node B (bottom 2 traces). It is evident that channel cross-talk noise in the SOA node A severely deteriorates the high signal lever in the eye diagram.

5. Conclusion

We have demonstrated successful routing of 10Gbit/sec optical packets through two complete nodes in the Data Vortex switch using bit-parallel WDM headers. This was facilitated by the use of LOA switching gates, which were shown to significantly reduce cross-talk among the WDM payload data channels. Control signaling between the two nodes was experimentally shown to properly route 10-packet sequences. The unique control mechanism effectively eliminates the need for packet contention resolution within the switch fabric, greatly simplifying the optical implementation of the system.

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