Optical Packet Switching through Multiple Nodes in the Data Vortex Architecture

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1. Introduction

Photonic switch fabrics have recently emerged in network elements for maintaining routed packet traffic in the optical domain and alleviating the electronic bottlenecks in today's fast growing communication and computing systems. We have recently proposed a new switching fabric architecture termed the Data Vortex that specifically enables implementation with optical technologies by avoiding the need for internal buffering [1,2]. The Data Vortex employs synchronous control signaling distributed throughout the fabric for packet flow control. The traffic control in the Data Vortex was demonstrated experimentally using two fully functional routing nodes [3,4]. In this paper, we demonstrate multi-hop routing through a 4–node Data Vortex switching fabric of WDM 10Gbit/sec packets. The header bits are encoded in a WDM bit-parallel fashion where every bit occupies a separate wavelength. This arrangement significantly simplifies the routing and reduces the overall latency.

2. Architecture and system configuration

The Data Vortex switch architecture consists of switching elements (i.e. routing nodes) arranged on a collection of concentric cylinders as shown in Fig. 1(a) [1]. Packets flow from the most outer cylinder to the most inner cylinder uni-directionally. Distributed control signaling is used to ensure that only a single packet enters a node in any given clock cycle.

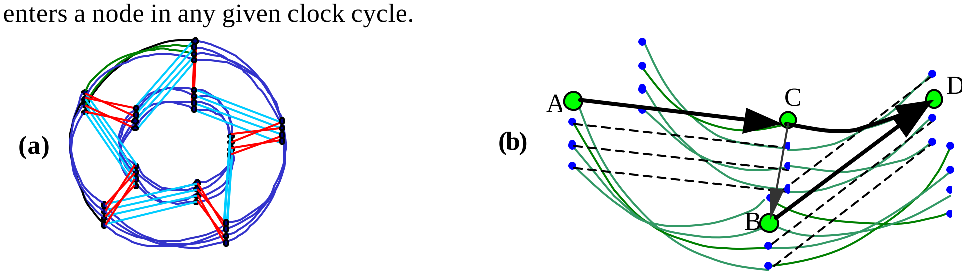

Fig.1. (a) Schematic of the Data Vortex topology with 2 cylinder and 5 angles. (b) Demonstrated Data Vortex sub-system. The large solid circles are the experimentally constructed nodes. The arrow from C to B indicates the control signal path. The arrows from A to C, C to D, and B to D are data paths.

We construct a Data Vortex sub-system that consists of 4 routing nodes, as shown in Fig. 1(b). Packets are injected into nodes A and B located at the outer cylinder. In accordance with the routing processor decision, packets from node A are then either dropped to routing node C located on an inner cylinder or simply deflected to another node on the same cylinder level. Likewise, packets entering node B may be either dropped to node D or deflected. At node C or D, packets can drop to the south ports, which lead to output interfaces, or deflect to remain at the same cylinder level.

In Fig. 2 the 4-node Data Vortex test-bed is shown. The node schematic shown in the figure inset consists of two semiconductor optical amplifiers (SOA), which form the switch element. Each packet is constructed with two header channels at λ_1=1550.9nm and λ_2=1537.3nm for header bits H_1 and H_2 such that (H_2H_1) represents the binary destination address. A framing channel at λ_3=1555.6nm is programmed to indicate the presence of a packet in the time slot. Two payload channels at λ_4=1545.3nm and λ_5=1553.3nm are encoded with data at 10Gb/sec. At each routing node only one of the header bits is decoded. Thus nodes A and B only decode the H_2-bit of the incoming packet using a 1nm band-pass filter centered at λ_2 and nodes C and D employ a filter at λ_1 to decode the H_1-bit. Filters at λ_3 in each node extract the frame bit information. The detected header and frame bits are used in the decision logic of the node routing processor to generate the appropriate drive signal for the SOA switches. The traffic control signals for node A, C, and D are programmed directly from PPG1 to allow flexible settings, while the control for node B is generated from the routing logic circuitry of node A. The latency of nodes C and D is set to be smaller than A and B to provide the proper delay to the control signal [4].

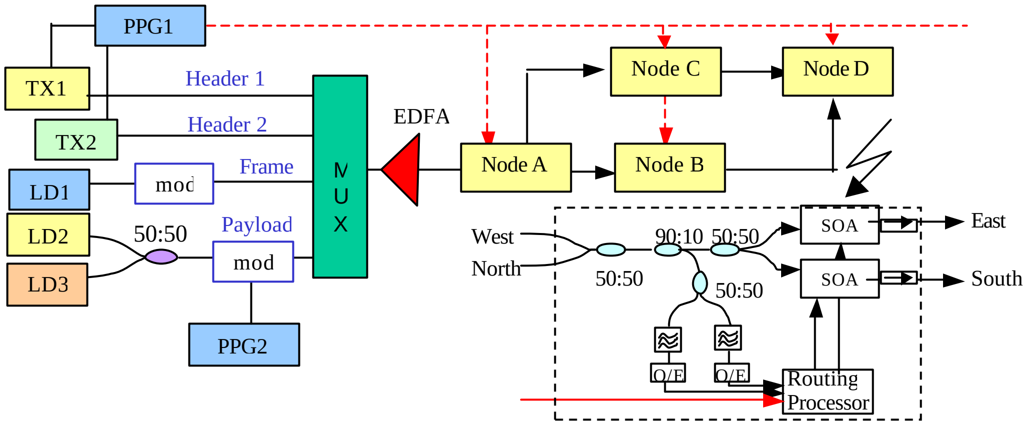

Fig. 2. Four-node routing test-bed schematic and node structure. PPG: pulse pattern generator; TX: transmitter; LD: laser diode; EDFA: Erbium doped fiber amplifier; SOA: semiconductor optical amplifier.

3. Results

To study the routing and control signaling mechanism under different traffic settings, we programmed a sequence of 20 packets, each carrying different routing destinations. The packets are 64ns long with a 6.4ns guard time. The guard time is programmed within the payload at the edge of the packet boundary to allow for the routing transients, as illustrated in the top trace of Fig. 3. The input packets into nodes A and B are provided with the framing sequence as shown Fig. 3(a). We randomly set the control sequence of node A to be “1010011011,1011111010”, node C to be “0110111010,0100010100”, and node D to be “0010101000,0100010010”, where “0” means “deflect” and “1” means "do not deflect" the message intended for the packet slot. Following the decoding of the packet target address bit and the control signal bit, the routing processor at node A determines if the packet will drop to node C through its south port. In a similar fashion, the routing processor of node C generates the control signal sent to node B to prevent packet contention at node D. In node D, the routing processor simply distributes all incoming packets to its output ports. Fig. 3(b) shows routed packets at the output ports of nodes C and D.

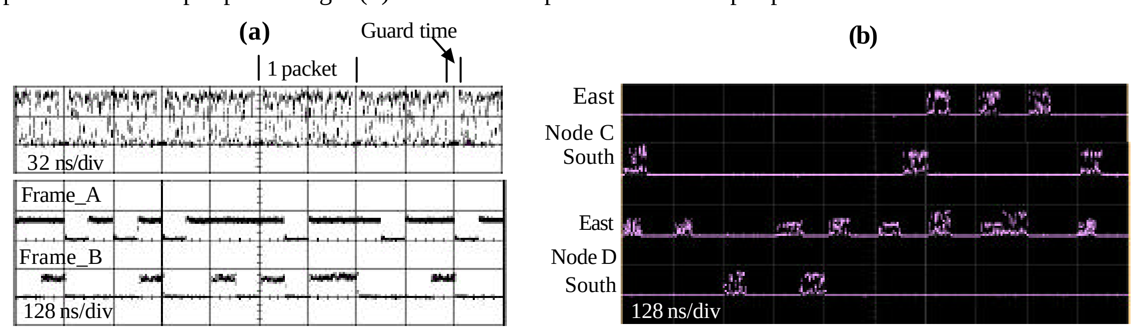

Fig. 3. (a) Input data to nodes A and B. (b) routing results out of nodes C and D.

4. Conclusion

Multi-hop routing of 10Gbit/sec optical packets through four complete nodes in the Data Vortex switch was demonstrated using bit-parallel WDM headers. Control signaling among four nodes was experimentally shown to properly route 20-packet sequences. The unique control mechanism effectively eliminates the need for packet contention resolution and buffering within the switch fabric, greatly simplifying the optical implementation of the system.

References:

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