Cascading switching nodes in data vortex optical packet interconnection network

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Cascading of semiconductor optical amplifier (SOA) based switching nodes has been studied experimentally in a re-circulating loop test-bed of the data vortex packet interconnection network. The experimental results show that the signal bit-error-rates can still exceed 10^{-9} after 72 node hops, demonstrating the physical layer scalability of the data vortex network.

Introduction: Ultra-high capacity optical interconnection networks are considered as a potential solution to the immense processor-memory access communications bottleneck, which is expected to dominate high-performance supercomputers [1, 2]. Optical packet switching fabrics have the potential to supply this next-generation technology with the performance characteristics necessary for efficient communications between supercomputer processor, memory and storage elements, even within systems containing thousands of such elements [3, 4]. The data vortex is one optical packet network designed specifically for large-scale processor-memory interconnections [5]. Its unique synchronous implementation and distributed control scheme not only eliminate the necessity for internal optical buffering, but also enable low switching latency and high throughput.

Most large-scale optical packet switches recently considered, including the data vortex, share the semiconductor optical amplifier (SOA) as the central active optical switch component. The potential benefits of the SOA-based switching elements are well known and include: high-speed switching, high extinction ratios, sizable operating bandwidth, and relatively compact footprint [6, 7]. It follows that the physical layer scalability of large SOA based switches will depend primarily upon the successful propagation of optical packets through multiple cascaded SOA elements. Recent simulations of the data vortex have shown that a moderately loaded interconnection network with over 10 k ports requires fewer than 45 node 'hops' for 99.99% of the injected packets [8].

Researchers have examined the performance of cascaded SOAs as in-line amplifiers in a transmission system both numerically and experimentally [9, 10]. Numerical studies on the performance of cascaded SOAs specifically configured as switching gates have shown that the initial signal dynamic range and the number of cascaded gates are the two critical system parameters [11, 12]. In this Letter, we demonstrate the routing of 10 Gbit/s optical packets through 72 SOA-based data vortex switching nodes in a re-circulating test-bed. The input power dynamic range can be greater than 15 dB for 50 cascaded nodes. The results indicate the potential physical layer scalability of the data vortex to port counts relevant for high-performance computing interconnection networks.

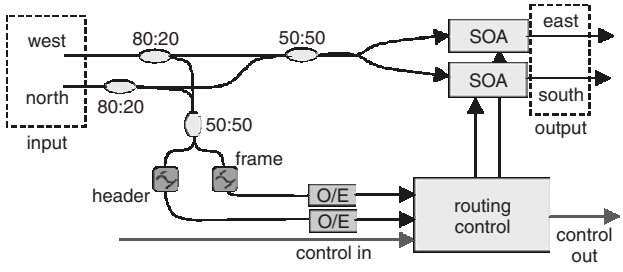

Fig. 1 *Data vortex switching node structure*

Data vortex switching node: The node structure is shown in Fig. 1. Each node has two input ports, west and north, and two output ports, east and south. At each input port, a small portion of optical power is tapped off by an 80/20 coupler to decode the header and frame information. The payload data is transparent and switched by the SOAs. The header and frame bits are converted to electronic signals and, along with the electronic input control signal from the inner cylinder node, are processed in the node control board. Accordingly, driving signals are generated to switch the SOAs on or off [5]. In the meantime, a control signal to the outer cylinder is also generated. The total latency, from the input port to output port, is approximately 4.3 ns.

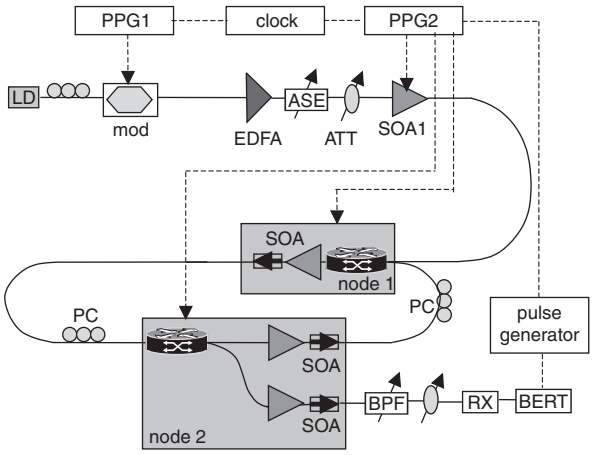

Fig. 2 *Experimental setup of switching-loop test-bed*
PPG: pulse pattern generator
LD: laser diode
EDFA: erbium-doped fibre amplifier
Optical path (solid line)
Electrical path (dashed line)
MOD: modulator
SOA: semiconductor optical amplifier
PC: polarisation controller

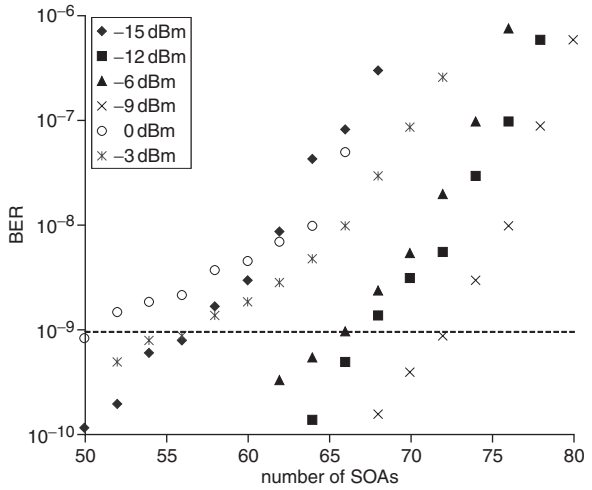

Fig. 3 *BER against number of cascaded SOAs*

Experiment: The experimental setup of the switching nodes re-circulating loop test-bed is shown in Fig. 2. A DFB laser at 1541 nm is encoded by a single $LiNbO_3$ modulator at 10 Gbit/s with a $2^7 - 1$ PRBS. The 32 ns long packet is formed by gating SOA1. Two such data vortex switching nodes are included in the 64 ns long re-circulating loop. Packets ingress from the west port of node 1. At node 2, the packet is either routed back to the loop through the east port or exits from the south port. In the experiment, the header and frame bits of each packet are always programmed as ONE. A control signal programmed into the multi-channel pattern generator (PPG 2) controls the loop switching. The SOAs are commercial devices (Kamelian OPB-10-10), which have a typical noise figure of 7 dB, unsaturated gain of 10 dB, and a saturation input power of approximately 0 dBm. In each node, the SOA gain is set to exactly compensate for the losses, which are approximately 4.5 dB. The modulation current driving the SOAs varies between 50–80 mA, depending on the input power. Such low driving currents eliminate the need for temperature controllers. To avoid the accumulation of noise in the loop, the SOA in node 1 is turned off when a packet is dropped from node 2. Since the packet size is short, as is typical in computing interconnection networks, the BERT must be externally gated by a pulse generator that is synchronised with PPG2. Fig. 3 shows the bit-error-rate dependence on the number of cascaded nodes and input optical power. The input power is defined as the average power, taking into account the 2.5% duty cycle of the packet which is injected into the loop once every 40 roundtrips. We tested the cascading performance by changing the input power from −15 to 0 dBm. With

the optimal input power of −9 dBm, a maximum number of 72 cascaded nodes is achieved with a 10^{-9} bit-error-rate. When the input power is high (larger than −6 dBm), the SOAs work in the saturation regime, leading to pattern dependent pulse distortion. With low input powers (< −12 dBm), the optical signal is quickly buried by noise due to mixing with amplified spontaneous emission. Fig. 3 also shows that with 50 cascaded nodes, which can support at least a 10 k × 10 k data vortex network, the dynamic input power range can be larger than 15 dB.

Conclusion: We have demonstrated the physical layer scalability of the data vortex packet interconnection network in a re-circulating loop experiment. The 10 Gbit/s optical packets can traverse 72 cascaded SOA-based switching nodes at a BER of 10^{-9} at the optimised input signal level. More than 15 dB of input power dynamic range was demonstrated with 50 cascaded nodes.

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References

1 Kleinrock, L., *et al.*: 'The supercomputer supernet testbed: a WDM-based supercomputer interconnect', *J. Lightwave Technol.*, 1996, **14**, pp. 1388–1399
2 Nishimura, S., *et al.*: '64-Gb/s highly reliable network switch (RHiNET-2/SW) using parallel optical interconnection', *J. Lightwave Technol.*, 2000, **18**, pp. 1620–1627
3 Papadimitriou, G.I., Papazoglou, C., and Pomportsis, A.S.: 'Optical switching: switch fabrics, techniques, and architectures', *J. Lightwave Technol.*, 2003, **21**, pp. 384–405
4 Focus Issue: High-capacity packet-switched fabrics, *J. Opt. Netw.*, 2003, **2**, (7)
5 Yang, Q., Bergman, K., Hughes, G.D., and Johnson, F.G.: 'WDM packet routing for high-capacity data networks', *J. Lightwave Technol.*, 2001, **19**, pp. 1420–1426
6 Olsson, N.A.: 'Lightwave systems with optical amplifiers', *J. Lightwave Technol.*, 1989, **7**, pp. 1071–1082
7 Hunter, D.K., Chia, M.C., and Andonovic, I.: 'Buffering in optical packet switches', *J. Lightwave Technol.*, 1998, **16**, pp. 2081–2094
8 Yang, Q., and Bergman, K.: 'Performances of the data vortex switch architecture under nonuniform and bursty traffic', *J. Lightwave Technol.*, 2002, **20**, (8), pp. 1242–47
9 Sun, Y., Srivastava, A.K., Banerjee, S., Sulhoff, J.W., Pan, R., Kantor, K., Jopson, R.M., and Chraplyvy, A.R.: 'Error-free transmission of 32 × 2.5 Gbit/s DWDM channels over 125 km using cascaded in-line semiconductor optical amplifiers', *Electron. Lett.*, 1999, **35**, pp. 1863–1865
10 Yu, J., and Jeppesen, P.: 'Improvement of cascaded semiconductor optical amplifier gates by using holding light injection', *J. Lightwave Technol.*, 2001, **19**, pp. 614–623
11 Woflson, D., Danielsen, S.L., Joergensen, C., Mikkelsen, B., and Stubjaer, K.E.: 'Detailed theoretical investigation of the input power dynamic range for gain-clamped semiconductor optical amplifier gates at 10 Gb/s', *IEEE Photonics Technol. Lett.*, 1998, **10**, pp. 1241–1243
12 Wolfson, D.: 'Detailed theoretical investigation and comparison of the cascadability of conventional and gain-clamped SOA gates in multiwavelength optical networks', *IEEE Photonics Technol. Lett.*, 1999, **11**, pp. 1494–1496