

# Ultra-high Capacity WDM Optical Packet Routing through an 8-node Data Vortex Sub-network

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**Abstract:** We demonstrate routing of 8-WDM-channel 10Gb/s optical packets through an 8-node sub-network of the Data Vortex, realizing virtual buffering within the switching fabric. Single pulse WDM encoding for the header simplifies packet control and reduces latency.

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## Introduction

Optical packet switching fabrics are emerging as critical technologies in network elements for high-speed data communication [1]. Maintaining routed packets in the optical domain offers the potential for exploiting WDM data encoding and realizing ultra-high throughput capacities. The key challenges facing the implementation of photonic switching fabrics include contention resolution and packet buffering, which often necessitate conversion to the electronic domain [2]. In particular, efficiently buffering an optical packet that contains data in several wavelength channels presents a severe practical challenge. Many switch fabric architectures that exhibit excellent performance in electronics fail to scale with optical data, requiring frequent conversions to electronics and back to optics. The architecture of the Data Vortex switching fabric has been specifically proposed to address the unique issues associated with optical packet switching [3,4]. To avoid packet contention, the Data Vortex employs a synchronous and distributed control mechanism for the packet flow. As a result, each node encounters at most one packet in a given clock cycle and no optical buffering is required to mitigate contention. This traffic control mechanism leads to packet deflection. However, the probability of multiple deflections for any one packet is minimized since packets are provided multiple paths to the destination [5]. An open path provided by the “angle” dimension of the architecture is always available to a deflected packet and thus provides a virtual buffering mechanism internal to the switching fabric.

Previously, we have experimentally demonstrated routing of optical packets through multiple hops of a single Data Vortex switching node [3]. The traffic control mechanism between two routing nodes was recently shown with WDM encoded optical packets [6,7]. In this paper, we report on an 8-node Data Vortex sub-network that demonstrates the critical fabric functionalities: packet generation and insertion through two input nodes that are interconnected to 6 routing nodes, packet flow control among two cylinder levels, packet deflection, and virtual buffering at the inner cylinder. The routed packets contain a data payload composed of 8 WDM channels and 10Gbit/s per channel. The packets’ header and framing bits are encoded in a bit-parallel WDM fashion to simplify the routing and to reduce latency. Each routing node includes two semiconductor optical amplifiers (SOAs) that switch the packets and compensate the loss in each node. The SOAs in each node consume only tens of mA of current, eliminating the need for temperature control. The power penalty incurred after the WDM packets traverse 7 nodes is shown to be approximately 1dB.

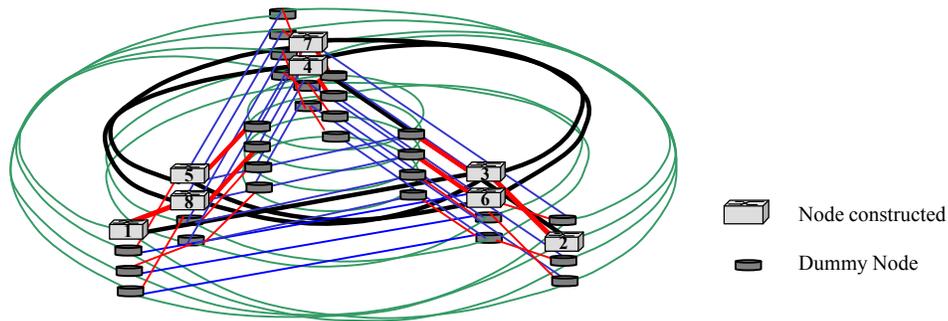


Fig. 1. Schematic of the Data Vortex topology with A=3, H=4, and C=3. Numbered square nodes are experimentally implemented.

**Data Vortex Architecture:** The Data Vortex switch architecture shown in Fig. 1 [3,4] can be described by three parameters,  $C$ ,  $A$ , and  $H$ , corresponding to the cylinder, angle and height parameters, respectively. Shown in Fig. 1 is a switching fabric of size  $C=3$ ,  $A=3$ , and  $H=4$  which would support 12 input and output ports. The number of cylinder levels ( $C$ ) scales as:  $C=\log_2 H+1$ . Each cross point shown is a routing node, which can be labeled uniquely by the coordinates  $(a,c,h)$ , where  $0\leq a<A$ ,  $0\leq c<C$ , and  $0\leq h<H$ . Data packets enter from routing nodes at the outermost cylinder and exit from nodes at the inner most cylinder. The innermost cylinder ( $c=\log_2 H$ ) also provides a virtual buffering function, allowing packets to circulate around when the output buffers are busy. The packet flowing between cylinders follows a binary tree such that the next most significant bit of the header address is fixed as packets are forwarded to the next inner cylinder routing level.

## Experiment

The arrangement of the experimentally implemented 8-node sub-network within the Data Vortex architecture is shown by the highlighted square nodes in Fig. 1. Fig. 2 details the experimental setup. Each packet consists of 2 header channels, 1 frame channel, and 8 payload channels. We use SOAs to modulate the header wavelength channels so that extinction ratios of larger than 40dB can be obtained. This prevents the rise of accumulated noise in the ZERO bit of the header address and avoids critical logic errors during the routing process. Nodes 1 and 2 are input nodes at the outer cylinder. Nodes 3 through 8 are routing and output nodes at the inner cylinder. Node 8 and node 3 provide control signals to node 1 and node 2, respectively, so that the contention at node 3 and node 4 is avoided. Control signals to nodes 3 through 8 are randomly generated by a multi-channel pulse pattern generator (PPG 1). In each node, 10% of the optical power is tapped off to extract the header and frame information. The control logic board processes the header, frame and control bits to generate the gating signals for switching the SOAs. The control logic board also produces a gating signal directed toward the appropriate outer cylinder node to prevent packet contention. Careful timing design is required, as this control signal must reach the outer node before the packet is processed. The total latency in each of the implemented nodes is 30ns. It is worth noting that the latency is dominated by optical delay due to long fiber pigtailed of individual components. If all the optical components were integrated into one chip, the optical delay can be substantially decreased. Taking into account the electrical delay of the control logic board, the overall latency of each routing node can be as low as 2ns.

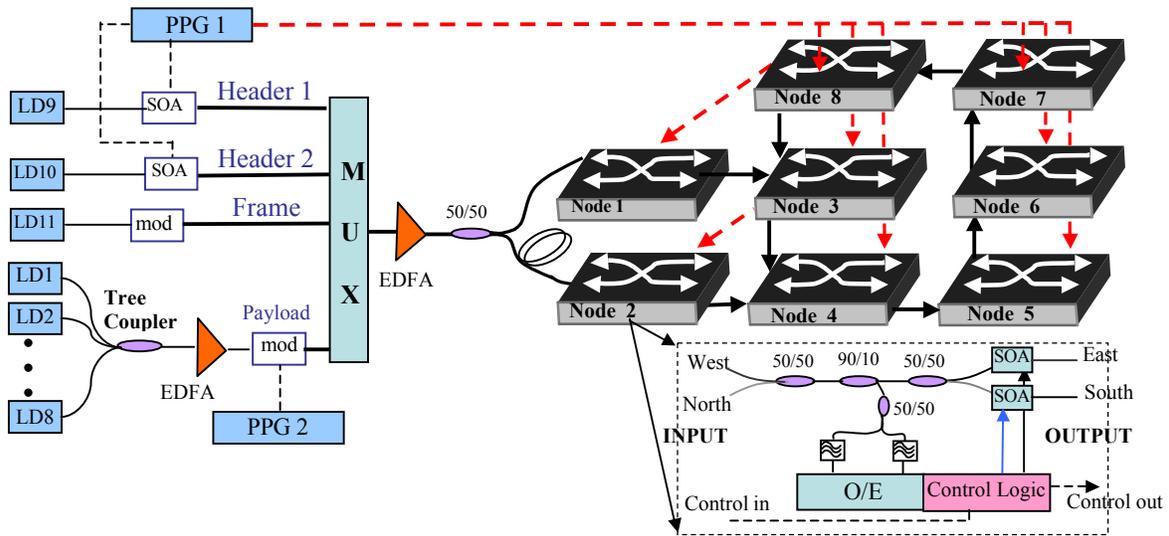


Fig. 2. Experimental setup of 8-node Data Vortex sub-network. PPG: pulse pattern generator; LD: laser diode; EDFA: Erbium doped fiber amplifier. Optical path (solid line); Electrical path (dashed line); Control line (bold dash); MOD: modulator; SOA: semiconductor optical amplifier.

The header and frame bits are encoded at separate wavelengths as single bits along the entire length of the 64ns long packet. To achieve low latency, these bits are stripped with simple wavelength filters and processed in parallel as the packet traverses through the node. Eight WDM payload channels, located between 1530nm and 1565nm, are encoded with 10Gb/s NRZ data streams. The bit pattern was  $2^9-1$  pseudo-random bit sequence. A guard time of 6.4 ns is inserted between adjacent packets, to allow for routing transients. We programmed a data sequence of 20 packets, each carrying routing destinations ( $H_2H_1$ ), as shown in Fig. 3(a). Although the packets payloads are continuously generated, packets with a ZERO frame bit are treated as empty and blocked at the input nodes. The packets injected through input node 2 are delayed relative to the packets at node 1 by 30ns, to achieve more

independent packet sequencing. Fig. 3(b) shows the routing results for one example routing sequence. In accordance with the generated routing destinations and frame bits there are 14 initial valid packets (with frame bits ONE) injected into nodes 1 and 2. Eight packets (P1 to P8) correctly propagate from node 1 to inner cylinder node 3, while the remaining six exit node 1 through its east port. As packets traverse node 3 and emerge from its east port toward the west port of node 4, node 3 sends a control signal to node 2 in order to prevent contention at node 2. As a result, only two packets (P9 and P10) of the 14 from node 2 drop to node 4. Packets then propagate from nodes 3 and 4 to nodes 5, 6 and 7 exiting along the way in accordance with their destination address. In the above sequence example the maximum number of hops any packet traveled is three. In order to test the virtual buffering capability of the Data Vortex we specifically programmed a sequence to let packets circulate through the test-bed inner cylinder. We then measured the bit-error-rate for the payload channels under three cases: back-to-back, after 1 hop at node 1, and after 7 hops at node 8. Fig. 4 shows the worst case results obtained with payload channel 8 at 1560.6nm. The power penalty after one hop is negligible, while a small power penalty of approximately 1 dB appears after 7 hops. The eye diagrams corresponding to error-free operation are shown as the insets in Fig. 4. For a large scale Data Vortex switching fabric (2k×2k), the average number of packet node hops is about 20 [5]. Thus, the node cascading results shown demonstrate the potential for successfully scaling the switch fabric.

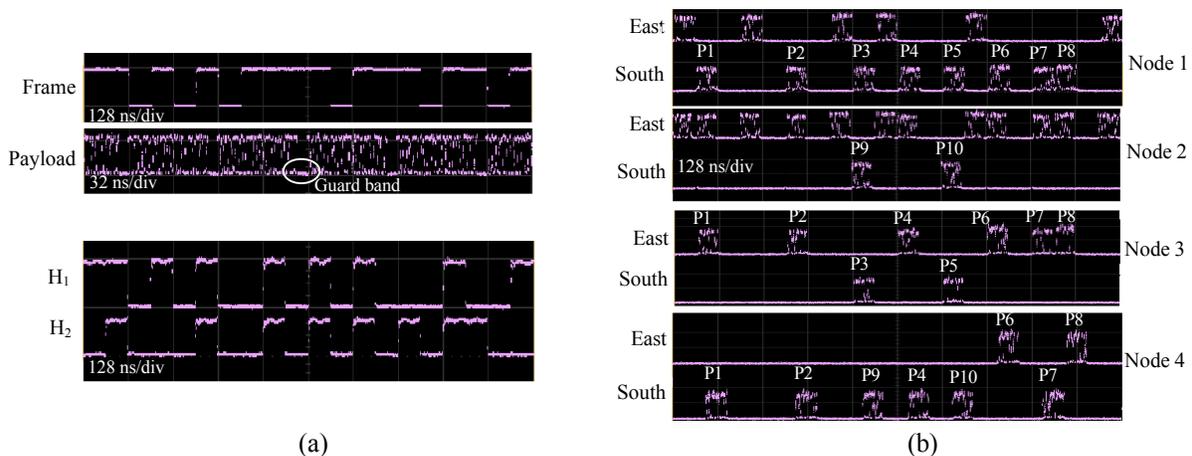


Fig. 3. (a) Data format of frame, headers and payload. (b) Routing results at four routing nodes. The top trace in each window shows the packets out from East port of the node and the bottom trace shows the south port of the node.

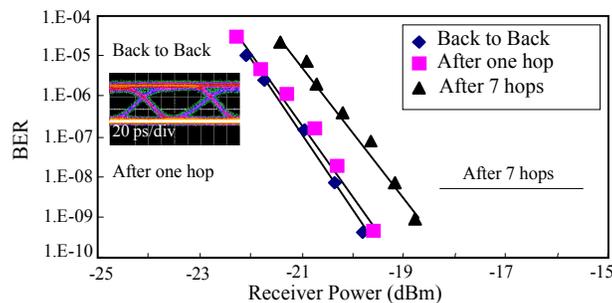


Fig. 4. Measured bit-error-rate performance for back to back and after 1 and 7 hops.

## Summary

Successful routing of optical packets through an 8-node Data Vortex sub-network demonstrates key functionalities of the switching fabric. Single pulse WDM encoding for the header and frame bits enables low latency and simplifies traffic control. Virtual buffering of the WDM packets is shown through 7 node hops incurring a power penalty of 1dB.

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