# A Wide-Band Photonic Packet Injection Control Module for Optical Packet Switching Routers

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***Abstract*—The implementation of a novel photonic injection control module that mediates packet injection into optical packet switching (OPS) routers is reported. Responding to a busy signal received from the OPS router, the module buffers the multiple-wavelength optical packets on a fiber delay line until a slot becomes available. The functionality of the module and its interoperability with a data vortex OPS router are demonstrated. Error-free (bit-error rate $< 10^{-12}$) routing of 80-Gb/s payload (eight wavelength-division multiplexing $\times$ 10 Gb/s) is confirmed.**

***Index Terms*—Multiprocessor interconnection, optical interconnections, optical packet switching (OPS), photonic switching systems, semiconductor optical amplifiers (SOAs).**

## I. Introduction

OPTICAL packet switching (OPS) is gaining wide acceptance as a potential solution for addressing the ultrahigh communications bandwidth demands and minimal latency requirements of next-generation high-performance computing systems as well as other system and local area network applications [1]–[3]. Bit-rate transparency and wavelength-division multiplexing offered by the optical domain present elegant solutions to the challenges faced by copper-based electronic networks at high data rates, namely increased power consumption, wiring density, and signal distortion over distances [4]. OPS systems, however, also present new design challenges that primarily rise from the fact that optical memory technology is still immature. Architectures that significantly limit buffer usage and utilize fixed-length fiber delay lines (FDLs) or other topological solutions to replace electronic random access memory have, therefore, been sought [3], [5]–[8].

Packet synchronization and injection control for OPS routers are key problems that have to be addressed before these routers become widespread [3]. Packets may only be injected when the OPS router is ready to receive them, to avoid internal contentions, and should, therefore, be buffered when the router is not ready. In time-slotted systems, packets also have to be synchronized with system slots. To avoid the cost and complexity associated with optical–electrical conversion, especially in multiple-wavelength systems, execution of these tasks in the optical domain is preferred [3]. Several optical solutions to the buffering and synchronization problems have been suggested. Feed-forward dynamically reconfigurable buffers [3], [9] can provide fine temporal resolution required for the synchronization, but become costly when scaled to longer delays on the order of the packet timescale. A novel compact module based on a series of fiber Bragg gratings combined with a widely tunable wavelength converter [10] has recently been proposed, but this module is limited in its design to processing single-wavelength packets.

The injection control module (ICM) [11] reported in this letter is intended to be placed at an input port of a slotted OPS router, where fixed-length packets (or cells) are used. It is designed to mediate packet injection into a router that has an internal contention resolution scheme, and therefore, exhibits marginal packet loss rates (PLRs) [5]–[7]. The ICM further reduces the PLR of these routers by reattempting the injection of rejected packets. For Bernoulli traffic, assuming that the initial PLR $(L)$ is low, the ICM reduces the PLR to $L^{n+1}$ if $n$ retransmissions are allowed [12].

The module is comprised of an FDL controlled by fast optoelectronic and electronic circuitry which facilitates the decoding of control signaling from the router to dynamically control injection on a packet-by-packet basis. Based on semiconductor optical amplifiers (SOAs), the ICM works at the packet timescale and can delay a packet until the router input port is available for injection. The maximum number of recirculation cycles is limited by the number of SOA hops that the optical signal can undergo while preserving its integrity. This limitation has been studied for similar SOA-based networks, and it has been shown that tens of hops can be traversed with minimal signal impairment [13]. The duration of a delay cycle can be set for a particular implementation, and should typically correspond to the slot time in the slotted OPS router. The module is also quite simple, utilizing only four SOAs, and its physical complexity is independent of the number of packet delay cycles.

## II. Architecture and Design

The ICM is based on a reprogrammable nonblocking $2 \times 2$ wide-band switching node that controls a feedback FDL (Fig. 1). The packets are encoded in the data vortex multiple-wavelength format [5], [14] where every packet is marked by an optical signal called *frame*, encoded on a dedicated wavelength, which remains constant for the entire duration of the packet. Other wavelengths are simultaneously encoded with address information required to route the packet in the switching fabric, and with the packet payload, segmented and encoded on multiple wavelengths.

The entire multiple-wavelength packet propagates as a unit through the router and the ICM. Group velocity dispersion and

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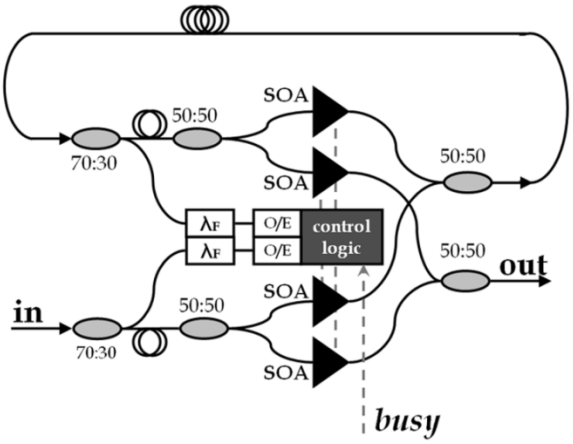


Fig. 1. ICM is comprised of SOAs, optical couplers (ellipses, with coupling ratios), filters ($\lambda_F$), p-i-n photodetectors (O/E), optical fibers, and an electronic control circuit.

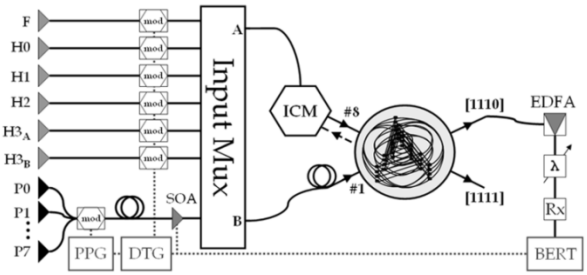


Fig. 2. Experimental setup. Eight payload DFB lasers (P0 through P7) are multiplexed, modulated (mod), and gated (SOA) to form the optical $8 \times 10$ Gb/s packets. Control channels $(F, H_i)$ are modulated, multiplexed with the packets, and injected into the ICM and an additional input port (#1) of the data vortex router. The ICM is connected to input port #8 of the router and receives an appropriate busy signal (dashed). The emerging packets are amplified (EDFA) filtered for wavelength selection $(\lambda)$, detected (Rx), and directed to the BER tester (BERT), which is synchronized with the PPG and the data timing generator (DTG).

resulting wavelength walkoff can be neglected as the propagation distances in question are limited to hundreds of meters for the largest scale systems.

Upon entry into the ICM, a portion of the packet power is tapped off, directed to a wavelength filter for frame extraction ($\lambda_F = 1555.75$ nm), and detected by a 115-MHz commercial p-i-n photodetector. This simple extraction and detection scheme using wavelength filters and slow photodetectors, facilitated by the wavelength-parallel structure [14], eliminates the need for complex header recovery circuitry. The resulting signals are then forwarded to the electronic control circuit implemented using a Xilinx complex programmable logic device (CPLD). The CPLD, with a latency of 4.9 ns, uses the frame bit extracted from the incoming packet and an electronic busy signal, received from the router, to make the routing decision. In the case where the busy signal is absent, the packet is injected into the router. If the busy signal is present, the packet is buffered on the FDL to reattempt injection in the following slot. The FDL length is designed such that the latency of a full pass through the module and the FDL corresponds exactly to the system slot duration, and the packet appears at the FDLs output exactly one slot time after it first entered the module.

At the beginning of the next time slot, another packet may be received at the input port and the control circuit makes a routing decision for both packets. If the busy signal is deasserted, to indicate that injection is now allowed, one packet is injected and the other is delayed. If the router port is still busy, one packet is dropped. The constant-value encoding of the frame wavelength maintains the inputs to the electronic circuit unchanged throughout the duration of the packet and facilitates the use of very simple and fast sequential circuitry. The busy signal also conforms to this convention by changing its state only during the deadtime between packets, as is done in the data vortex router [14].

Four transparent fiber-optic paths in the module connect the module input port and the FDL output to the module output port and the FDL input (Fig. 1). The routing decisions are executed by four SOA gates, driven by commercial laser drivers. The SOAs (Avanex A1901) are chosen for their fast switching speed ($<$1 ns) and their relatively flat gain curve over the $C$-band. Their 8.5-dB gain (at a drive current of approximately 50 mA) allows for full compensation of the coupling losses.

The injection module is comprised of two submodules: 1) a passive optics assembly that contains filters, couplers, and optical fibers; and 2) a printed circuit board on which the SOAs, photodetectors, and electronics are mounted. The slot time for the system is 38.4 ns, and the module latency and FDL length are designed accordingly. The latency of the passive optics submodule is 22.0 ns, and the total latency of the electronic decision circuit, the photodetectors, and SOA pigtails is 16.4 ns.

This paradigm for integration of wide-band SOA switching elements, along with electronic decision circuitry and simple control information extraction techniques, has been shown to be an attractive solution for OPS systems [14]. The injection module, therefore, supports the high optical bandwidth of multiple-wavelength packets while maintaining its independent control mechanism and optical transparency.

## III. Experimental Results

Bit-error rate (BER) and power penalty analysis of the ICM were reported in [11]. In this letter, the interoperability of the ICM with OPS systems is experimentally demonstrated by using a previously constructed $12 \times 12$ data vortex OPS router [14]. Two router input ports (#8 and #1) and two router output ports ($[1110]$ and $[1111]$, denoted by their four-bit addresses) are used. The ICM is connected to input port #8, and receives a corresponding busy signal.

An experimental setup that constructs data vortex packets and analyzes them as they emerge from the router (Fig. 2) is employed. Eight distributed feedback (DFB) lasers, with wavelengths ranging from 1536.7 to 1558.2 nm, are multiplexed, modulated with $2^7$-1 pseudorandom bit sequence at 10 Gb/s using a pulse pattern generator (PPG), decorrelated by approximately 450 ps/nm with 25 km of a single-mode fiber. The decorrelated streams are then gated by an SOA to form discrete packets. The frame and header wavelengths are modulated with the packet control information using $LiNbO_3$ modulators, and are then multiplexed and aligned with the gated packet payloads in a passive input optical multiplexer. The input multiplexer is designed so that packets share the frame signal and the three most significant bits of the header. The least significant bit of the header $(H_3)$ is driven separately for each input port to allow for addressing of separate packet flows to separate router output ports.

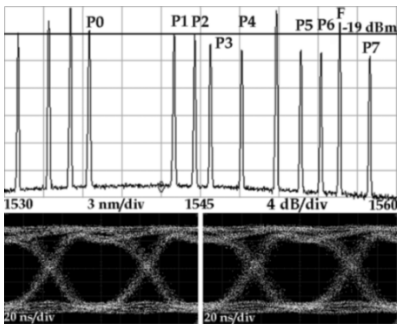


Fig. 3. Spectrum (top) of the optical packets as they emerge from the router's output port $[1110]$. The frame $(F)$ and payload $(P_i)$ wavelengths are annotated. The reference level represents the packets' average power. The rest of the wavelengths carry the data vortex internal routing header. Eye diagrams at of the input (left) and the output (right) at $\lambda = 1544.74$ nm.

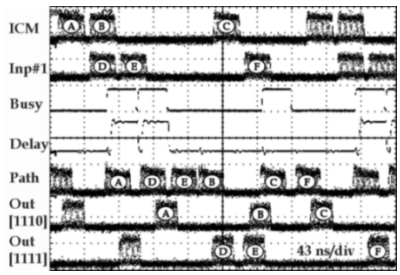


Fig. 4. Signals (top down: optical ICM and port #1 input signals, electronic *busy* and *delayed* signals, the merged stream of optical packets on the shared path, and output ports $[1110]$ and $[1111]$) show that packet $B$ is delayed by the ICM when the busy signal is received, thus avoiding contentions with packets $D$ and $E$ on the shared path. Packet $B$ then appears at its output port with a two-slot delay. The optical packets are represented by one of the eight payload wavelengths, selected by a wavelength filter.

The constructed optical packets are launched into the ICM. Packets are also injected into input port #1, after being delayed by one time slot (38.4 ns), in a manner that emulates the delay of an additional ICM. The packets' power levels (Fig. 3) are consistent with the data vortex router packet format and stay well below the SOAs saturation level: The total packet power is $-7.5$ dBm, whereas the input saturation power for the SOA is approximately 0 dBm.

Upon emerging from the router, the packets are amplified by an erbium-doped fiber amplifier (EDFA), filtered for wavelength selection, detected by a 10-Gb/s p-i-n receiver, and directed to a BER tester which is synchronized with the PPG and gated for packetized data. BER measurements are conducted on each of the eight payload wavelengths individually.

A packet pattern is created to demonstrate packet buffering in the presence of busy ports (Fig. 4). In this pattern, three packets (annotated $A, B, C$) are transmitted into the ICM and are addressed to output port $[1110]$. Three additional packets $(D, E, F)$ are injected into input port #1 and are addressed to output port $[1111]$. Each packet is 35.2 ns long, and they are spaced by 3.2 ns to form 38.4-ns-long slots. Due to the structure of the data vortex, the routes taken by these packet flows share internal paths [5], [14]. To avoid internal contentions on these paths, a busy signal is emitted for input port #8, triggered by packets $D$ and $E$.

Responding to the received busy signal, the ICM buffers packet $B$ (i.e., sends it to the FDL) twice and only then injects it into the router. The fifth line of Fig. 4 shows the traffic on the internal fiber shared between the two flows: Packet $B$ is delayed and is transmitted on the fiber only after packets $D$ and $E$, as expected. The optical signal ejected from output port $[1110]$ shows that packet $B$ is indeed delayed by two slots. The optical signal from port $[1111]$ is identical to the optical signal injected into input port #1, except for the 148-ns routing delay. This demonstration of a two-cycle delay confirms, under the abovementioned assumptions, that the ICM can be used to reduce the PLR of a router from $L$ to $L^3$.

Error-free transmission of the packets routed through the ICM and the data vortex router is also verified. A BER of $10^{-12}$ or better is measured on all eight payload wavelengths. The BER measurement is performed on packet $B$, which takes the longest path through the network: two delay passes in the ICM and four node hops in the router [14].

## IV. Conclusion

The design and fabrication of an ICM for OPS routers has been reported, and its functionality has been verified. The correct interoperability with an OPS router serves to demonstrate the module's ability to resolve contentions in optical networks. This illustration of a wide-band FDL-based packet injection module has, thus, shown it to be useful as a fundamental functional subsystem for OPS routers.

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