Error-Free Operation of an All-Silicon Waveguide Photodiode at 1.9 µm

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Abstract: Error-free detection at 1 Gb/s is demonstrated with a Si ion-implanted waveguide photodiode operating at 1.9 µm. The measured 0.14-A/W responsivity corresponds to a 5 dB decrease in photocurrent compared to operation at 1.55 µm.
OCIS codes: (040.6040) Silicon; (040.5160) Photodetectors

1. Introduction

High-traffic networks and telecommunication systems requiring increased optical link capacity have propelled the search for ways to increase link aggregate bandwidth. Recent advances in long-wavelength technology [1] have shown that additional wavelength bands can be utilized to increase data throughput [2], including the demonstration of 10 Gb/s data transmission at 1884 nm [3]. However, these long-wavelength (> 1.7 µm) signals also pose an inherent challenge for detection due to the fact that they are beyond the band edge of many common detector materials [4,5]. Bandgap engineering using super lattices [6] provides some solutions for detection at these longer short-wave IR (SWIR) wavelengths but requires significant engineering effort. However, long-wavelength data reception beyond the U band can be achieved utilizing extrinsic photodectors (PDs), where ion implantation is used to induce sub-bandgap absorption in Si waveguides using a straightforward fabrication process at very low cost.

Here we report the experimental demonstration of a Si waveguide PIN PD device with long-wavelength absorption induced by sub-bandgap defect states formed *via* Si^+ ion implantation [Fig. 1(a)-1(b)]. These detectors have previously been shown to have bandwidths of > 35 GHz, responsivities up to 0.8 A/W [7] and error-free data transmission of 10 Gb/s at wavelengths near 1.55 µm [8]. In this report, we demonstrate error-free operation (BER < 10^{-9}) of a 2-mm-long PD with 1 Gb/s data rates at 1.9 µm. To the best of our knowledge, this is the first systems-level demonstration of a monolithic Si waveguide PD operating at wavelengths beyond 1.8 µm.

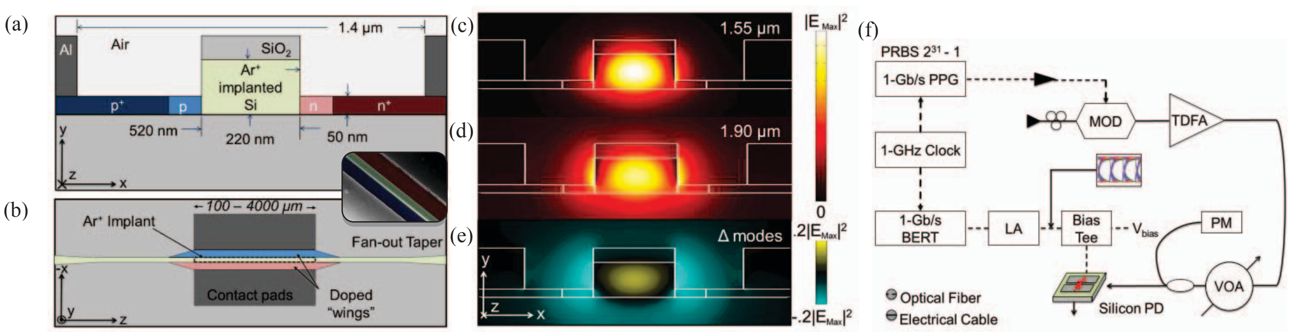

Figure 1. (a) PD cross-section shown with dimensions and doping profiles given in [7] (inset) false color SEM of PD, (b) top view of PD, (c) 1.55 µm mode profile, (d) 1.9 µm mode profile, (e) difference between 1.55 µm and 1.9 µm, (f) experimental setup.

2. Results

The Si^+ implanted Si waveguide PIN PDs were fabricated on the CMOS line at MIT Lincoln Laboratory, as described in [8], with dimensions given in Fig. 1(a) and Fig. 1(b). As shown in Fig. 1(f), 1 Gb/s non-return-to-zero (NRZ) data is generated by a pulse pattern generator (PPG), and used to drive a $LiNbO_3$ modulator, which imparts the signal onto a 1.9 µm carrier. The modulated optical signal is then sent to a thulium-doped fiber amplifier (TDFA), and a variable optical attenuator (VOA) is used to control the power being launched on-chip for BER measurements. A 1% power tap after the VOA diverts a portion of the signal to an optical power meter (PM) for input power monitoring. The PD is contacted with electrical probes rated for 40 GHz operation, and a bias tee is used to apply a DC bias. The electrical data signal is connected to a limiting amplifier (LA) through the AC port of the bias tee, and the signal from the LA is

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sent to either a bit-error-rate tester (BERT) or digital communications analyzer (DCA) for eye diagram measurements [Fig. 2(c)].

Our measurements demonstrate error-free operation of a 2 mm device at 1 Gb/s with a 25V bias, and of a 3 mm device at 0.975 Gb/s with a 25V bias. Eye diagrams measured at the LA output for the 2 mm device are shown in Fig. 2(c) with variable input power. The top eye is open both vertically and horizontally, corresponding to error-free operation at 13 dBm input power. The bottom eye operates at half the power of the top eye, and is near closing in the vertical direction, which corresponds to a higher BER. The PD 3-dB bandwidth is measured to be .995 GHz, limiting the data rate. The on-chip detector sensitivity (corresponding to a BER of 10^{-9}) is estimated to be -4.4 dBm for the 2 mm device, accounting for a measured facet loss of 12.6 dB.

Photocurrent versus V_{bias} is also measured at both 1.55 µm and 1.9 µm and shown in Fig. 2(b). An approximate 5.1 dB decrease in photocurrent is measured for long-wavelength operation with $V_{bias} > 5$ V. The decrease in confinement factor [Fig. 1(c)-(e)] of the optical mode accounts for 2 dB of the penalty but can be addressed with proper waveguide design. The responsivities at 15 V for both 1.55 µm and 1.9 µm are found to be 0.46 A/W and 0.14 A/W respectively, accounting for facet loss. These results are lower than previous results for similar devices at 1.55 µm [7,9], suggesting that higher responsivities are possible with proper device conditioning as discussed in [7].

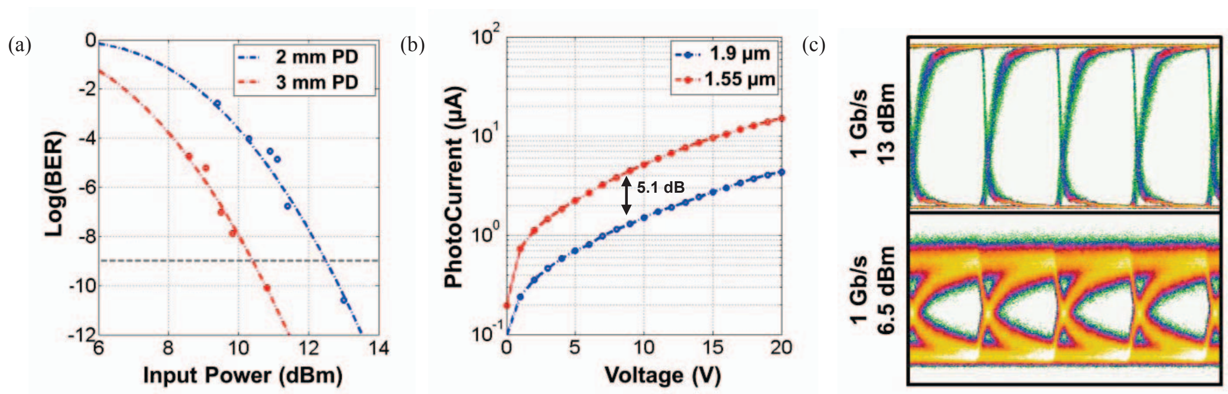

Figure 2. (a) BER curve for 2mm and 3mm devices, 25V bias, operating at 1 Gb/s and .975 Gb/s respectively, (b) Photocurrent of a 2 mm device (c) Eye diagrams for 1 Gb/s with 13 dBm and 6.5 dBm input power.

3. Conclusion

Error-free data reception at 1 Gb/s for an all-Si PD operating at 1.9 µm has been achieved with an estimated sensitivity of -4.4 dBm. A 5.1 dB penalty in photocurrent was observed compared to operation at 1.55 µm and responsivity was found to be 0.14 A/W for a 15 V bias. Higher data rates can be achieved by increasing the frequency response through better contact pad design and the use of shorter devices. Sensitivity can also be improved through a number of design considerations including larger waveguide dimensions for higher optical confinement at 1.9 µm, proper device conditioning as mentioned in [7], and/or utilizing an avalanche waveguide PD structure [10].

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