ME3.2 (Invited)
14:00 – 14:30

A 30 GHz Silicon Photonic Platform

Multi-Project Wafer Shuttles for Next-Generation Optical Systems

Matt Streshinsky[3,4], Ari Novack [3,4], Yang Liu[1], Ran Ding[1], Michael Gould[2], Tom Baehr-Jones[1], Qi Li[5], Yisu Yang[1], Yangjin Ma[1], Yi Zhang[1], Kishore Padmaraju[5], Keren Bergmen[5], Andy Eu-Jin Lim[3], Guo-Qiang Lo[3], and Michael Hochberg[1,3,4]

[1]*Department of Electrical and Computer Engineering, University of Delaware, Newark, DE, USA*
[2]*Department of Electrical Engineering, University of Washington, Campus Box 352500, Seattle, WA 98195, USA,*
[3]*Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 11 Science Park Road, Singapore Science Park II, Singapore 117685*
[4]*Department of Electrical and Computer Engineering, University of Singapore, Singapore*
[5]*Department of Electrical Engineering, Columbia University, 500 West 120th Street, New York, New York, USA*

***Abstract*—Shared shuttle run services are ideal for rapid and relatively inexpensive prototyping. We present a silicon photonic platform that offers monolithically integrated modulators and photodetectors with 30 GHz bandwidths, available through the OpSIS MPW service.**

Keywords—Electrooptic modulators; microwave photonics; nanophotonics; photodetectors; silicon

I. Introduction

Driven by the surge in mobile users connecting to the Internet via smartphones, tablets and what is being called the "Internet of everything," the data center is emerging as a hotbed of innovation for optical interconnects and switching architectures. Several distinct opportunities exist, ranging from top-of-rack aggregation applications (500+ meter reach) to adjacent or next-nearest-neighbor interfaces (few meters) to intra-rack and board-to-board (~1 meter), to MPU-to-memory interfaces (potentially few-centimeters). As the distance gets shorter, naturally the aggregate bandwidth requirement increases, and the energy-per-bit requirements become more stringent, thus making it harder for photonics to compete; generally speaking photonics is more competitive at longer distance scales, due to the low losses of optical fibers. A number of papers have been written about the practical issues of addressing these various kinds of challenges [1-4]. A number of solutions have been proposed, ranging from photonic interposers to VCSEL based links to DML and EML laser-based solutions, wavelength multiplexing (WDM), and polarization control and multilevel signal encoding such as PAM [5-7].

Photonics are beginning to be extensively utilized in HPC type applications, and interconnects are projected to account for a rapidly increasing fraction of the cost of supercomputers [8]. This will likely also be the case for high-end data centers over the coming years, given the relatively low utilization fractions in current data center applications [9].

Interesting features of data centers and HPC systems include their relatively short service lifetime—typically only a few years—and their relatively tight environmental controls. This makes them a prime candidate for rapid photonics innovation, since Telcordia and IEEE standards are mainly irrelevant in large, high-end HPCs. Furthermore, because of the need for relatively short links, it is possible for solutions using relatively exotic fiber plants to be economically practical. Relatively expensive fibers, such as multicore, polarization maintaining, erbium-doped, and hollow-core fibers all can be used for relatively short-distance runs, and some of these solutions alleviate various shortcomings of integrated silicon photonic solutions. Furthermore, the relatively short service lifetime and large scale of data centers lends itself to customized interconnect and switching solutions—being able to rapidly prototype and develop bespoke photonic solutions for these applications has great value to the community. We present an open platform, available through the OpSIS MPW foundry service [10], in which this type of innovation can occur.

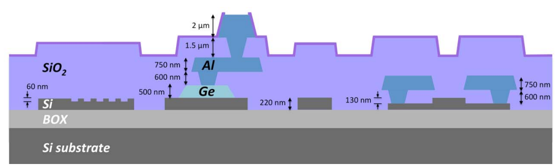

Fig. 1. Cross section of grating couplers, photodetectors, waveguides, and modulators available in the platform.

II. Fabrication

Fabrication occurred at the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. The starting material was an 8-inch silicon-on-insulator wafer with 220 nm top silicon layer, 2 µm buried-oxide layer and standard resistivity silicon substrate. The individual fabrication steps are similar to those presented in [11]. A 60 nm anisotropic dry etching was first applied to create the grating couplers. Then, the rib and channel waveguides were formed by further etching steps. The p++, p, n, and n++ implants for the Si modulator and the p-type doping for anode formation of the Ge p-i-n photodetectors were performed, followed by a rapid thermal anneal at 1030 ºC for 5 s to activate the dopants in Si. Ge was then selectively grown to a thickness of 500 nm. The growth region was defined by etching a window in SiO_2 masking layer. Ion implantation was then performed for the Ge regions. The annealing recipe for dopant activation in Ge was 500 ºC for 5 min. The fabrication process was completed with the formation of contact vias and aluminum interconnects. The schematic cross-section without the details of metallization steps is shown in Fig. 1.

III. Device Characterization

A. *Grating Couplers, Waveguides, and Y-Junctions*

In this platform, low loss grating couplers, waveguides, and Y-junctions have been successfully demonstrated. Non-uniform grating couplers exhibited an average insertion loss of 3.1 dB at 1550 nm and a 50 nm 1.5-dB bandwidth. The average waveguide loss for 500 nm rib waveguides with a 90 nm slab is 1.5 ± 0.6 dB/cm. Routing waveguides consisting of a 1.2 µm wide channel were measured to have losses of 0.27 ± 0.06 dB. Finally, Y-junction devices show average insertion losses of 0.26 ± 0.01 dB per Y-junction.

B. *Gain-Peaked Germanium p-i-n Photodetectors*

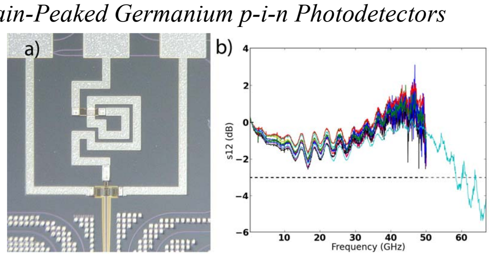

Fig. 2. (a) Micrograph of gain-peaked photodetector. (b) EO response of a several photodetectors up to 50 GHz and a single high-speed measurement showing 58 GHz bandwidth.

Germanium photodetectors were fabricated with an inductive metal loop in order to enhance the bandwidth, as described by [12]. Fig. 2(a) shows an optical micrograph of one of the devices. At a 2 V reverse bias, an average responsivity of 0.71 ± 0.031 A/W and average dark current of 3.42 ± 0.38 µA was measured. Fig. 2(b) shows EOS21 performance with bandwidths exceeding 50 GHz.

C. *Ring and Traveling Wave Mach-Zehnder Modulators*

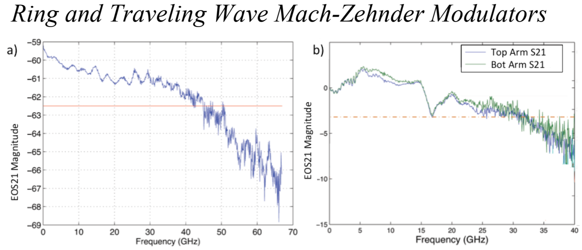

Fig. 3. Typical EOS21 performance of the (a) ring and (b) TWMZ devices showing 3dB bandwidths of 40 and 30 GHz, respectively.

Ultra-high speed ring modulators and traveling wave Mach-Zehnder modulators are also demonstrated in this platform. 12-µm radius dual-bus ring modulators with a lateral PN junction were tested for bandwidth. The "through" port was used as the output. These devices were measured to have a free spectral range of 7.65 nm, Q factor near 2.8k, tunability of 28 pm/V, and 3-dB bandwidths near 40 GHz. A typical ring transmission spectrum at 0 V bias is shown in Fig. 5 and an electrooptic S21 trace is shown in Fig. 3(a).

The TWMZ devices use 33Ω coplanar transmission line electrodes with the RF mode matched to the optical velocity. DC V_π was measured to be 7.0 V for a 3 mm long device. The EOS21 of this device is shown in Fig. 3(b), with a 3dB bandwidth of 30 GHz. Eye diagrams were also taken using the TWMZ device. Fig. 4 shows two different 40 Gb/s eyes using a drive voltage of 2.5 V_{pp} and 1.6 V_{pp}, achieving 5.1 dB and 3.1 dB extinction with 1.7 and 1.4 dB of excess loss, respectively.

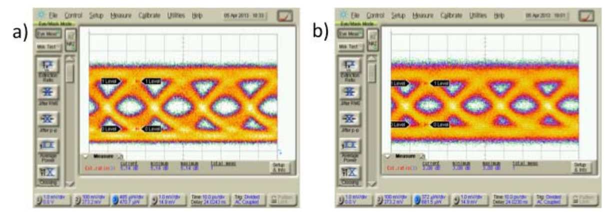

Fig. 4. 40Gb/s Eye-diagrams of a differentially-driven TWMZ with: (a) 0.25 V bias and 2.5 V_{pp} drive voltage, (b) 0 V bias and 1.6 V_{pp} drive voltage.

IV. Conclusions

We present the first silicon platform with integrated 30 GHz modulators and detectors. Low loss passive and high-speed active device performance suggests that this platform is suitable for building complex integrated photonic systems-on-chip for data center applications.

Acknowledgment

The authors would like to thank Gernot Pomrenke, of the Air Force Office of Scientific Research, for his support under the OPSIS, PECASE, and STTR programs, and would like to thank Mario Paniccia and Justin Rattner, of Intel, for their support of the OpSIS program.

References

[1] D. Miller, Proc. IEEE, vol. 97, no. 7, pp. 1166-1185, 2009.

[2] Y. Vlasov, "Silicon photonics for next generation computing systems", in *European Conf. Optical Communications* (Brussels, Belgium, 2008)

[3] T. Baehr-Jones *et al.*, Nature Photon., vol. 6, no. 4, pp. 206-208, 2012

[4] G. T. Reed and A. P. Knights. *Silicon photonics*. Wiley, 2008.

[5] L. Li, *et al. IEEE* 62nd *Electronic Components and Technology Conf*, 2012, pp. 1040-1046.

[6] A. Alduino and M. Paniccia, Nature Photon., vol. 1, no. 3, pp. 153-155, 2007

[7] M. Paniccia, M. Morse, and M. Salib, "Integrated Photonics," in *Silicon Photonics*, Springer Berlin Heidelberg, 2004, pp. 51-88.

[8] P. Pepeljugoski, *et al. Optical Fiber Communication and the National Fiber Optic Engineers Conf.,* 2007, pp. 1-3

[9] L. A. Barroso and U. Holzle, Computer, vol. 40 no. 12, 2007, pp. 33-37.

[10] http://opsisfoundry.org/

[11] T.-Y. Liow *et al.*, IEEE J. Sel. Top. Quant. Electron, vol. 16 no. 3, 2010, pp. 307-315

[12] M Gould *et al.*, Opt. Express, vol. 20, 2012, pp. 7101-7111