# On the Design of a 4×4 Nonblocking Nanophotonic Switch for Photonic Networks on Chip

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*Abstract:* **The architecture of a 4×4 nanophotonic switch element based on silicon microring resonator technology is introduced. The internally nonblocking design provides an optimal building block for photonic network on chip architectures.**

## Introduction

The recent trend toward chip multiprocessors (CMPs) in modern high performance computing architectures has highlighted the need for a low latency, high-bandwidth, power efficient intrachip communications infrastructure. Packet-switched on-chip global communications networks have been proposed as a solution to this apparent communications bottleneck [1]. Thus, an increasingly larger proportion of the design space for future CMPs must be dedicated to the construction of an on-chip interconnection network. However, as power dissipation continues to be the ultimate limiting factor in contemporary processor designs, *performance-per-watt* becomes the defining figure of merit for the next generation of high-performance microprocessor architectures.

The need for an interconnect solution that provides low latencies and high bandwidths while maintaining minimal power dissipation can be met by leveraging the unique advantages provided by photonics. Due to the inherently high bandwidth-distance product of photonic communication links and the bit rate transparency of optical switching elements, power scaling can essentially be decoupled from link distance and interconnect bandwidth, respectively. Thus, the possibility of nanophotonic networks on chip (NoCs) dramatically disrupts the current trend of power scaling in multiprocessor architectures by offering power savings of up to two orders of magnitude over comparable electronic networks [2].

Recent advancements in nanoscale silicon photonics bring the integration of complete, functional photonic systems integrated using standard VLSI technologies closer to fruition [3]. The ability to integrate photonic devices in standard CMOS processes is an important prerequisite to the viability of a photonic NoC in real-world multiprocessor computing systems. While the implementation of an all-optical NoC is intractable due to the immaturity of processing and buffering in the optical domain, architectures have been introduced which circumvent these disadvantages via hybrid electronic/photonic designs [4].

## Nanophotonic Switch Architecture

The switching node is the atomic building block of all interconnection network architectures and is thus a primary consideration in the design of any network. Therefore, a nanophotonic switch compatible with the aforementioned hybrid network paradigm is required. The physical limitations imposed by integration necessitate a compact, low loss design, while maintaining a maximum level of functionality for application in photonic on-chip interconnection network architectures.

The fundamental photonic switching element utilized in the design of the nonblocking switch is shown schematically in Fig 1a. The structure consists of a microring resonator positioned adjacent to a waveguide intersection. Switching is achieved through resonance modulation via carrier injection into the ring. High performance silicon microring resonator based modulators
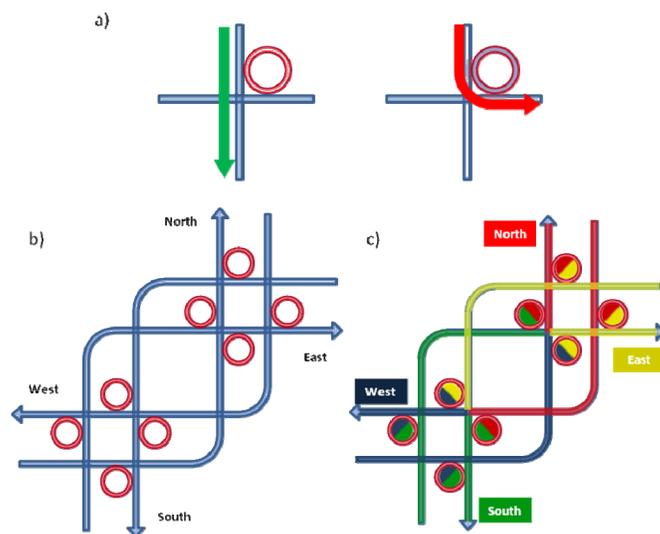


**Fig. 1**: Schematic of a 4 × 4 Nonblocking Nanophotonic Switch

capable of photonic switching have been experimentally demonstrated [5].

Using the fundamental switching element introduced above, a spatially minimal, fully functional 4×4 nonblocking nanophotonic switching node can be constructed as shown in Fig 1b. The compactness and symmetrical nature of the node design allows for the efficient layout and implementation of various network topologies on an integrated platform. The switch design employs a minimum number of ring resonator devices (8) to provide the desired switching functionality while avoiding internal message contentions. This is achieved through the provisioning of exactly one ring per necessary switched path and non-overlapping internal paths from each input to every other output port of the node. The independence of the message paths is highlighted in Fig 1c.

Simpler architectures for a 4×4 photonic switch, with limited functionality, have been introduced [4]. However, it has been shown that the performance ceiling of a ultra-high bandwidth hybrid on-chip interconnection network is dominated by the latency of the electronic message routing procedure [6], which is directly correlated to the size of the network dimensions and to the complexity of the employed routing algorithms, both of which increase dramatically with decreased switching node functionality. Thus, the availability of an atomic nonblocking 4×4 switching element, allowing for the implementation of a nonblocking network topology, is critical in achieving the maximum performance to complexity ratio in various photonic NoC designs.

## References

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