Transparent, Low Power, All-Optical WDM Interface for High Performance Digital Systems

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Abstract: **We demonstrate a scalable WDM optical interface with 70% improvement in power efficiency over traditional methods. Serial 40 Byte packet streams are transparently mapped onto a WDM optical signal with a measured power penalty of 1.5 dB.**

Introduction

The recent emergence of chip multiprocessors (CMPs) for driving performance via increases in the number of parallel computational cores has accelerated the bandwidth requirements in high-performance processors [1]. With vastly growing numbers of cores and on-chip computation, communications on-chip and most critically off-chip has become the key bottleneck limiting system performance. Traditional electronic communications infrastructures have, unfortunately, been unable to provide the necessary bandwidth demanded by high performance computing nodes while maintaining manageable power consumption figures.

Optical interconnects offer a potentially disruptive technology solution by providing ultrahigh bandwidths via WDM, while delivering lower latency and power consumption over comparable electronic solutions [2]. However, as off-chip bandwidth demands of CMPs continue to increase (a current generation Cell processor can maintain 50.6Gbytes/s [3]), the power dissipation associated with bandwidth scaling via parallel electro/optical links grows rapidly due to the cost of multiple signal conversions.

In this work, we propose and demonstrate a scalable and transparent interface approach that directly maps serial streams of electronic packets onto multiple WDM channels in a highly power efficient manner. By requiring only one optical modulator, one broadband gate and one optical receiver regardless of the number of WDM channels utilized the optical interface is able to achieve significant power savings. We report a 70% improvement in the static power dissipation in the following demonstration. The experiment involves the translation of serial 40Byte PCI Express (PCIe) encoded electronic packets onto an 8-channel WDM optical link with a measured power penalty of 1.5 dB [4].

Power Consumption Reduction

Standard parallel optical links require a set of drivers, optical modulators, photodetectors, transimpedance and limiting amplifiers, and other related circuitry (e.g. for thermal stability) per optical channel, regardless of whether they exist on individual waveguides or WDM. Thus, dissipated power is typically a linear function of the number of channels employed in the system.

The transparent optical interface introduced here uniquely partitions serial packets onto multi-channel WDM packets while employing only one modulator/receiver pair. In this scheme, the dynamic power, which is proportional to the modulation frequency, remains the same as in the standard parallel optical interface, but the static power dissipation, which is proportional to the number of devices, is significantly reduced by a factor corresponding to the number of WDM channels.

Transparent WDM Interface Design

A schematic of the transparent WDM interface is provided in Fig. 2. Electronic data streams originating from the processor simultaneously modulate each wavelength (W0 to W7) using one high-speed optical modulator (MOD), effectively mapping the data stream onto multiple WDM channels. Each modulated wavelength is then filtered using 100 GHz thin film filters (TFF) and appropriately delayed with respect to each other using optical fibre delay lines (FDL) by an amount of time corresponding to the WDM packet segment length, which is determined by the connected optical interconnection network. All wavelengths are then multiplexed onto a single fiber. A second broadband optical modulator (Gate) precisely gates the WDM time-shifted optical signals to create the wavelength parallel packets shown in Fig. 3. For a multi-lane serial protocol such as PCIe, the time-compressed wavelength-striped data from each lane is interleaved in a time-slotted manner (Fig. 3) on the same fiber. At the destination core, the serial electronic packet is optically reconstructed by filtering and delaying each wavelength in an inverse manner. The WDM channels are finally multiplexed onto one fibre prior to the DC-coupled broadband receiver (RX), thus enabling the reconstruction of the original serial streams of electronic packets.

Experimental Evaluation

In our demonstration, serial 8b/10b PCIe formatted streams of 40 bytes are modulated at 2.5 Gbps and mapped onto 8 WDM channels spaced by 0.8 nm (1543.72 nm to 1549.33 nm), producing 5 byte WDM subpackets electronic packet [5]. A reduction of 73.5% in the static power dissipation (for a system with 8 optical channels) was achieved when taking into account the broadband optical modulator. The power penalty of the transparent WDM interface was measured to be 1.5 dB ($BER < 10^{-12}$) (Fig. 4) with respect to a back-to-back link with the entire electronic packet encoded onto one WDM channel (W0). The source of the power penalty is attributed to the variations in power and extinction ratio across the WDM channels under a fixed receiver voltage threshold.

Conclusions

A scalable and transparent WDM optical interface was demonstrated with 70% improvement in the static power efficiency. PCIe encoded electronic packets of 40 Bytes were mapped onto 8-channel WDM optical link with a power penalty of 1.5 dB. The low-power WDM interface efficiently addresses the growing off-chip bandwidth demands of high performance computing systems.

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References

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[2] Miller, Prof. IEEE, (2000), pp. 728-749.
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[4] Liboiron-Ladouceur, *et al*. LEOS, WEE7 (2007)
[5] Liboiron-Ladouceur, *et al*. OFC, JWA59 (2007)

Appendix of Figures

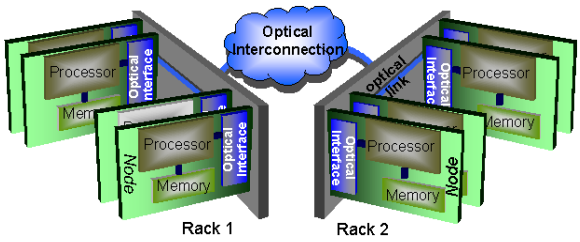

Fig. 1: *Transparent optical WDM interface for inter-node communications infrastructure.*

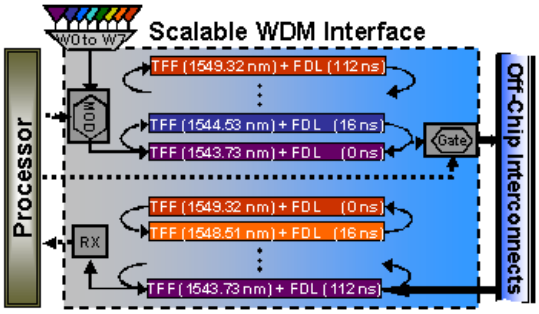

Fig. 2: *Schematic of the transparent WDM interface for off-chip communications.*

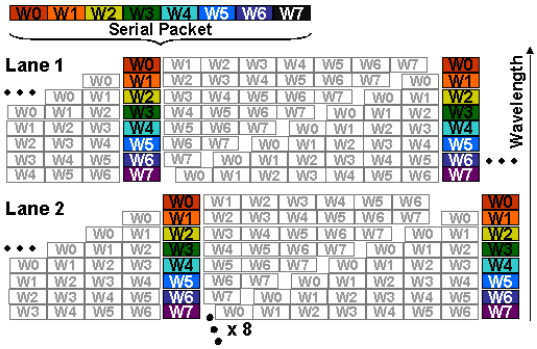

Fig. 3: *Serial electronic packets onto multiple WDM channels (W0 to W7).*

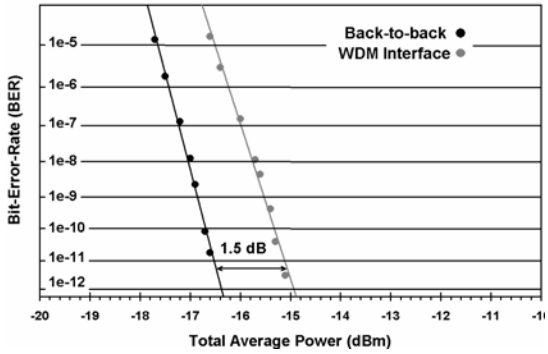

Fig. 4: *Measured power penalty of the interface.*