WDM Routing in Photonic Packet Switch

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With rapidly increasing data rates in both computing and communication systems, optical packet switches are emerging as potentially attractive high-bandwidth solutions to the electronic bottleneck [1][2]. In this paper we present a photonic packet switch that is based on a novel architecture named Data Vortex. The Data Vortex has been proposed as an internal low latency interconnection network for high-speed computer systems [3]. Its architecture, shown in Fig.1, is geometrically arranged as a system of connected concentric cylinders. Packets generally travel in a given direction around the network entering at the most outer cylinder and exiting at the most inner cylinder where the output ports are located. Each routing node indicated by a circle in Fig.1 consists of two input ports that can accept packets from an outer cylinder (North input) or from the same cylinder (West input); and two output ports that can connect to the next inner cylinder (South output) or to another node on the same cylinder (East output).

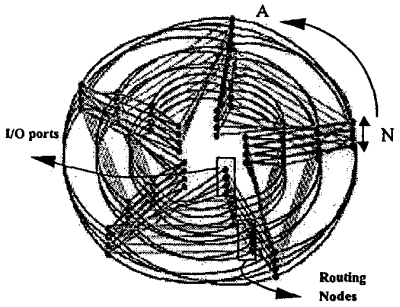

Fig.1. Data Vortex architecture with N=4, A=5

The Data Vortex dimensions are defined in terms of the cylinder height, N, and the number of angles, A, around the cylinder. A network with X ports will be constructed with cylinders of height N=X and A that is chosen to be a small odd number, typically 5. The number of cylinders scales as: $C=\log_2(N)+1$, and the total number of routing nodes is thus: $AN(\log_2(N)+1)$. The packet header is decoded in a binary tree fashion as it propagates from the outer to the inner cylinders, so that the total number of bits in the header address is $\log_2(N)$. Each header bit is encoded by a unique wavelength, and simple wavelength filtering can be used to extract the address information at specific cylinders. The last cylinder provides temporary output buffering and identifies exit angle. To avoid the difficulty of optical buffering, only one input packet is permitted to enter a node in any given clock cycle. This is realized by adding control lines between competing nodes from the inner cylinder to its outer cylinder neighbor. Numerical studies of the traffic flow in the Data Vortex architecture have shown that the architecture can be scaled to 10k port sizes while sustaining high throughputs and low latencies [4].

To demonstrate the routing functions of the Data Vortex and measure the physical layer performance we constructed a routing node test bed [4]. The propagation of packets through multiple node hops is emulated by configuring the test-bed in a re-circulating fashion. The experimental setup is shown in Fig.2.

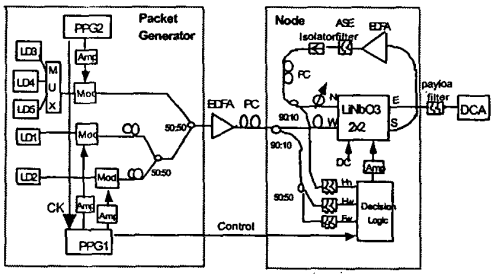

Fig.2. Experimental setup of the node test-bed

In the Packet Generator section shown, 2 CW lasers LD1 and LD2 at 1547nm and 1551nm are modulated by programmed framing and header sequences from the Pulse Pattern Generator or PPG1. The modulated optical framing and header are aligned with their corresponding optical payload each consisting of three WDM data channels at 1552nm, 1553nm and 1555nm from LD3, LD4 and LD5. The packet length is set to be 32ns including a 4.8ns guard-time band that allows for the switching transients between edges of packets. Each packet's three-channel WDM payloads are modulated by a pseudo-random pattern at 10Gibt/s from PPG2, which also generates a synchronous clock for PPG1. An EDFA is used to compensate the losses through the modulating and multiplexing stages.

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The routing node is simply constructed with a single $LiNbO_3$ crossbar switch. A Polarization Controller (PC) is inserted at the input to compensate the polarization sensitivity of the switch. The re-circulating configuration is achieved by connecting the output of the node (the South port) back as the North input. The initial packet sequence is programmed to keep only one packet entering the node in any given packet clock cycle. Within the loop, an EDFA with ASE peak filtering is used to compensate the losses through the switches and through the taps and splices. The header and framing bits are tapped, filtered and converted to electronics feeding into the decision logic circuitry. Also feeding to the node decision logic is the corresponding control signal generated by PPG1. Depending on the associated destination and control condition programmed, each of the packets will re-circulate through the node a varying number of times. A packet sequence entering the test-bed will therefore emerge out of order since different packets took a varying number of hops through the node. As an example, we tested a 40-packet sequence given by " 0010, 1110, 1101, 0111, 1010, 1110, 0000, 0000, 0000, 0000", where "1" represents a full packet slot while "0" is an empty packet slot. According to specific header address and control for each packet, the expected output packet sequence is: " 0000, 1010, 1111, 0101, 1100, 0000, 0000, 0000, 0001, 1111". As shown in Fig.3, the experimental results are consistent, demonstrating correct multi-hop performance by the node test-bed.

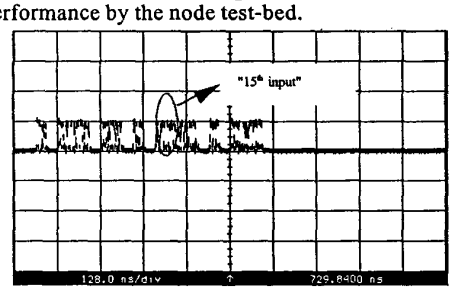

Fig.3. (a) Input packet sequence with 4-packets/div

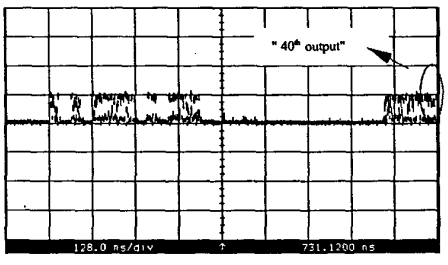

Fig.3. (b) Reordered output sequence of 40 packets

To verify the successful routing function we examine the detailed payload of each packet from input to output. For example, the 15^{th} packet in the input sequence is programmed to travel through 6 node hops and arrive as the 40^{th} packet at the output sequence, shown in Fig.3. The end portions of this 15^{th} input packet and corresponding 40^{th} output packet are shown to match in Fig.4.

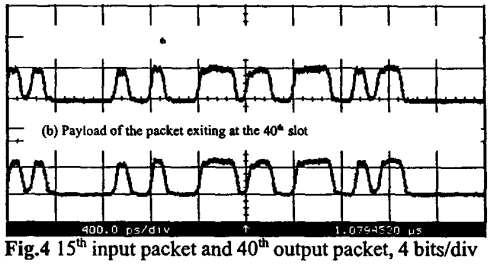

Fig.4 15^{th} input packet and 40^{th} output packet, 4 bits/div

The resulting eye diagrams are given in Fig.5. The output shows the collective eye diagrams of all the packets that have propagated through varying number of node hops. For a maximum of 6 node hops we find clean and open eye diagrams.

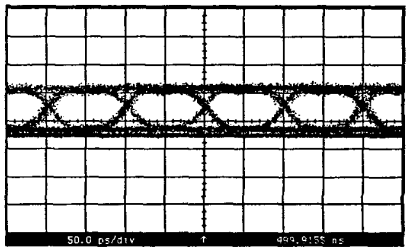

Fig.5 (a) Eyediagram of input packets

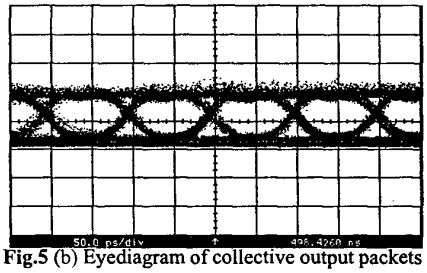

Fig.5 (b) Eyediagram of collective output packets

Reference:

[1]Yoshiharu Maeno et al, IEEE Photonic Technology Letters, Vol.10, No.8, 1998

[2]Yasuo Shibata et al, IEEE Journal of Lightwave Technology, Vol. 16, No. 12, 1998

[3] J.Cohen, NASA Insights, No.71998, pp2-11

[4] Q.Yang et al, Optics in Computing 2000, pp.555, SPIE, Vol.4089