Single-wire DAC/ADC Control and Feedback of Silicon Photonic Ring Resonator Circuits for Wavelength Switching

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Abstract: We develop a robust and scalable solution for control and feedback of silicon photonic circuits used for optical unicast and multicast. A single-wire DAC and ADC feedback architecture is evaluated with 20Gb/s PAM-4 data streams.

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1. Introduction

As Silicon Photonic technology matures, fabrication foundries are able to integrate optical components for chip scale communications [1]. The foundries support a library of components including Mach-Zehnder modulators (MZM), spatial switches, optical splitters and photo-detectors. Among these, the micro-ring resonator (MRR) is one of the most versatile building blocks with a narrow wavelength selectivity. Along with modulation capabilities, the MRR allows wavelength filtering, hence applicable for (de)multiplexing the wavelength division multiplexed (WDM) signals at a small footprint and low energy consumption [2]. However, MRR resonance characteristics make it susceptible to deviation from the optimal operations. Thermal variations can shift the resonance and cause high optical losses. A common method to address these problems is an integration of a micro-heater next to the MRR to “tune” the local temperature and fix resonance to the desired wavelength. An analog feedback loop [3] can tap a portion of the optical signal dropped from the MRR and adjust the bias on the heater to maximize the transmission power. However, a digital interface is still needed for a selective wavelength operation. While Digital feedback solutions [4-6] can achieve both functionalities, they rely on traditional digital-to-analog (DACs) and analog-to-digital converters (ADCs), which require a large number of parallel input/output (I/O) pins. For example, a 4-channel receiver [4] with 8-bit DACs and 16-bit ADCs requires 24 I/O pins for each MRR and 96 in total. In [5], the number of ADCs was reduced in a cascaded MRR structure, however tens of I/O pins are still required for multiple DACs.

In this work, a single digital I/O for control and a single digital I/O for feedback purposes is implemented to replace conventional DACs and ADCs to reconfigure the MRR device. It provides a scalable solution while maintaining reliable and desired wavelength switching operations. Our proposed single-wire DAC/ADC architecture is also compatible with a robust feedback tuning algorithm that is implemented on a field-programmable gate array (FPGA). By utilizing pulse-width-modulation (PWM) digital signals, this novel control and feedback strategy achieves unicast and multicast functionalities with 20Gb/s four level pulse amplitude modulation (PAM-4) optical data streams.

2. Single-wire DAC and ADC architecture

![Fig. 1. (a) Schematic of digital-to-analog and analog-to-digital control and feedback (b) Transient response of digital-to-analog circuit (red curve) and MRR thermal-optic response due to a changed duty cycle of the PWM control signal.](image)

Fig. 1 shows the building blocks for realizing the wavelength switching and feedback for reliable operations of an MRR. On the control side, a PWM control signal is generated by the FPGA and converted to bias voltage to tune the resonance of the MRR. On the feedback side, the analog feedback signal coming from the MRR is also converted back to a PWM signal for the FPGA to process. Based on the input and the output PWM signals, the feedback control algorithm implemented as a finite-state-machine (FSM) will tune the resonance of the MRR for optimized operations.

The digital-to-analog converter is implemented for the control side. By increasing/decreasing the duty cycle of the PWM control signal, the bias voltage on the heater is increased/decreased. The PWM generator first generates the
signal at 1.2MHz, which passes through the converter consisting of a comparator, a low-pass filter and a buffer for driving the current to the MRR heater. Fig.1 (b) shows the digital-to-analog circuit and MRR response time are 620µs and 30.3µs due to a duty cycle change from 29.67% to 42.26%. The time response of the circuit is 5 times faster than the MRR, which guarantees a fast tuning procedure. The clock frequency of the FPGA at 625Mhz provides a 9-bit resolution (625M divided by 1.2MHz) with a single wire.

For the feedback, a portion of the optical signal is tapped from the MRR and converted to an analog signal at the photo-detector (PD). The signal then passes through the analog-to-digital converter consisting of a comparator and a triangular wave generator. The analog signal from the PD is compared with the triangular wave at 150KHz, resulting in a feedback PWM signal, received by the reader, also at 150KHz. The resolution of our analog-to-digital converter is 12-bit (625Mhz divided by 150KHz), with only a single wire required.

The single-wire ADC/DAC structure is also compatible with the feedback control algorithm for tuning the MRR to maximize transmission power in unicast and divide power equally in multicast operations. The algorithm starts with an estimate of the PWM control signal that sets the bias voltage for each required operation. However, due to thermal fluctuations, the resonance may shift and need to be fixed to the desired wavelength. To achieve this, the algorithm first detects the sign of gradient [6] at the estimated duty cycle of applied PWM signal, and tunes the resonance based on expected operations as well. For unicast, the algorithm keeps increasing/decreasing the duty cycle in steps until the maximized transmission power is achieved. For multicast, the algorithm begins with the last participating MRR to maximize the dropped power, and all other participating MRRs in the cascaded structure waits until the preceding MRR is finished. They are then tuned to drop optical power that is equal to the first tuned MRR. The transient operation of the feedback tuning procedures is presented in the results section.

3. Experimental Setup

![](image)

The experimental setup is shown in Fig.2. The proposed control and feedback architecture is evaluated with two cascaded MRRs for unicast and multicast. A tunable laser (TL) is set to a specific wavelength on the C-band. A 10Gb/s pseudo random bit sequence (PRBS) is generated using a programmable pulse generator (PPG). The positive output data (D) is attenuated by 6dB and negative data (D̅) output is phase-matched with an electrical delay line (ED). Subsequently, D and D̅ are combined by a combiner and amplified using an RF amplifier to drive the MZM to generate the 20Gb/s PAM-4 signal. The polarization controller (PC) is used to set the maximized optical signal to the SiP Chip.

An FPGA configures each MRR with bias voltage through the single-wire DAC and ADC. Two additional I/O pins from the FPGA are used in multicast operation. An optical splitter is used to tap 10% of the optical power to a PD feeding it back to the FPGA at each output port of the MRRs. The other 90% is amplified by an erbium doped fiber amplifier (EDFA) to compensate for the ~15dB fiber to grating coupler loss. The optical PAM-4 signal is directed to a digital communication analyzer (DCA) for capturing the eye-diagram and estimating the symbol-error rate (SER).

4. Results

![](image)

Fig.3. (a) Transient responses for uncasting of MRR#1. (b) Corresponding spectrums and eye diagrams of MRR#1 before and after tuning. (c) Transient responses for uncasting of MRR#2. (d) Corresponding spectrums and eye diagrams of MRR#2 before and after tuning
Fig. 3 shows the experimental results of two unicast cases. The resonance of MRR#1 is 6dB deviated from the input wavelength at 1547nm (Fig. 3 (a)). An increased duty cycle of applied PWM signal is required. The optical transient response (blue curve) is captured in the PD and the feedback process starts at \( t = 37 \mu s (t_2) \) and ends at \( t = 271 \mu s (t_1) \). The PWM signal received by the FPGA is shown in black, where the duty cycle gradually increases from 27.24% at \( t = t_0 \) until the feedback algorithm detects a negative change and returns to the maximum point where the duty cycle stays at 92.78%. The orange curve shows the applied voltage on the MRR heater during the tuning operation. The applied PWM control signal and its duty cycle are shown in the black box. Fig. 3 (b) top illustrates the resonance of MRR#1 versus the input wavelength before and after tuning. Eye diagrams are also shown at the bottom. The corresponding SERs are 2e-6 and 7e-18. The results for MRR#2 is collected with input wavelength at 1560nm are shown in Fig. 3 (c) and (d). In this scenario, a decreased PWM duty cycle is needed. The tuning procedure takes 218 \( \mu s \) in total and achieves ~3dB increased optical power. The corresponding received PWM duty cycles are 50.26% at the beginning and 96.20% at the end. The applied PWM’s duty cycle decreases from 64.41% to 61.77% during tuning. MRR#2’s resonance versus the input wavelength are shown at the top of Fig. 3 (d). The resulting eye diagrams are shown at the bottom and SERs are 2e-7 and 3e-18.

Fig. 4 shows the experimental results for the multica.sting data at 1547nm through both MRRs simultaneously. The feedback operation as captured in the PDs is shown in Fig 4(a) (blue and orange curve). The feedback starting at \( t = 17 \mu s (t_2) \) is completed in 327\( \mu s \). At \( t = 228 \mu s (t_1) \), the resonance of MMR#2 (the last participating MRR) reaches the input wavelength where maximum output power is obtained and the algorithm starts to tune MRR#1. Multicast is achieved as MRR#1 drops the same optical power as MRR#2 at \( t = 344 \mu s (t_2) \). The applied PWM and its duty cycle for both MRRs is labeled in the black box. Fig. 4 (b) shows the transient of received PWM signals. During the tuning procedure, the duty cycle of PWM received signal from MRR#2 (in the top of Fig 4 (b) ) is 27.24\%, 71.01\% and 49.21\% at \( t_0, t_1, \) and \( t_2 \). The transient of the received PWM signal from MRR#1 is shown at the bottom of Fig 4 (b), with the duty cycle increasing from 29.28\% at \( t_1 \) to 50.77\% at \( t_2 \). The resonances of MRR#1 and MRR#2 are shown in the green and purple curve before tuning and the eye diagrams for detuned MRR#1 and MRR#2 are shown at the bottom with SERs of 2e-9 and 2e-7 (Fig 4 (c)). After tuning, SERs are improved to 2e-12 and 3e-11 for MRR#1 and MRR#2. The eye diagrams and resonances corresponding to input wavelength are shown in Fig. 4 (d).

5. Conclusions
We show that the single-wire ADC/DAC architecture can achieve wavelength switching for unicast and multicast with 20Gb/s PAM4 optical signals. The ADC/DAC conversion speed is optimized for micro-second scale, and it is shown that thermo-optic response is the limiting factor for the feedback operation. The demonstration validates that our novel control and feedback strategy has the potential for deployment in scalable and reliable SiP subsystems.

6. References