Application Details for Embedded Digital Test Core: Optoelectronic Test Bed and Wafer-level Prober

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Abstract

A multi-purpose digital test core utilizing programmable logic has been introduced [1,2] to implement many of the functions of traditional automated test equipment (ATE). While previous papers have described the theory, this paper quantifies the results and presents additional applications with improved methods. The digital test core provides a substantial number of programmable I/O for testing circuits and systems. It may be used either to enhance the capabilities of ATE or to provide autonomous testing within large systems or arrays of components. This technique has been expanded upon to produce greater functionality at higher frequencies.

Based upon limitations of current ATE and BIST, the need for the digital test core is described. The test core concept is reintroduced within an opto-electronic pattern generator and sampler. The performance of the device is discussed, and then a second application of the digital test core is introduced as a nano-scale wafer-level embedded tester.

1. Introduction

Modern automatic test equipment (ATE) has continued to increase functionality along with performance, however the pace of future development is undetermined. With increasing costs and test design integration, future devices may soon be limited in development by the test equipment available. Relentless advances in logic performance continue to follow Moore's law, resulting in ICs with more functionality and higher speeds. I/O rates measrue in hundreds of megabits per second on wide data buses, and on-chip clocks commonly exceed 2 GHz. When combined with optics, serial data rates are approaching 10Gbps. Faster data rates are inevitable.

The trend of electronics packaging continues to provide a higher pin density between the logic devices and the next level of systems. Incorporation of nanoscale structures within these pins will lead to densities of several thousand per cm^2 in the short term, and perhaps to ~100,000/cm^2 in the not-to-distant future[2].

Electronic applications will benefit greatly from these properties of future devices, but at the same time creating difficult challenges for testing. Electrical probe capabilities are stressed even with pin denstities of 1000/cm^2. The highest performance ATE available today barely meets the needs of current devices, supporting data rates of only 3.2 Gbps. But these testers come at a price of several thousand US dollars per channel, so a 1,000 channel ATE costs several million dollars. Projected prices of ATE systems in the future extend to the $50 million range by 2010 [3]. Additionally, these systems are not expected to be scalable to handle higher-performance devices [4].

The question is how can testing keep pace with the electronics trends of the future? The advantage of ATE is its ability to test a wide range of different devices, but at a high cost. Built-in self-test (BIST) can reduce the number of test pins needed and reduce cost, however it generally requires added silicon area and significant design effort. As devices become smaller and packaged to nano wafer level devices, BIST reaches a point where it is a greater hindrance than benefit. Since ATE and BIST each has its own advantages and limitations, a top-down approach can be taken to designing a new testing strategy.

In previous papers, the idea of a new approach to testing was introduced [1,2]. This concept was called the Digital Test Core (DTC). A field-programmable gate array (FPGA) is used as both the pin electronics and the interface the test computer. Together with the high speed multiplexing techniques [5], data rates can be increased well into the gigahertz range without relying upon expensive ATE hardware. By extending the support logic to encompass a broad range of functions in a standalone digital test core, test instrumentation cost can be minimized while improving functionality and performance.

This paper presents the effectiveness of this approach by providing the results of two separate high-performance applications: an opto-electronic interface to transmit and receive high speed test signals, and a nano-scale wafer-level prober. Both applications make use of the digital test core to provide a high-speed interface with multiple test functions.

In section 2, the concept of the Digital Test Core is explained in detail. The features and application possibilities are described. In section 3, an opto-electronic test bed is presented with the performance results. Section 4 concludes by describing the current effort to produce a nano-scale wafer-level prober. It make use of the Digital Test Core to provide high-speed (~4.8Gbps) test vectors to multiple devices on the wafer. This application is desgined to be scalable for the number of devices on the wafer.

2. Digital Test Core Concept

The digital test core is a reusable, reconfigurable circuit that can be incorporated into various testing scenarios to enhance current test capabilities or to employ new test functions. The DTC includes programmable logic to produce test stimuli and capture output responses through programmable I/Os. Also a provision is made for a large test vector memory. When coupled with additional logic to provide multi-gigahertz speeds and a Universal Serial Bus (USB) bridge to a controlling computer, a miniature tester is created to interface to the device under test.

A block diagram for the digital test core is shown in Figure 1. The programmable chip at the center of the digital test core is a Xilinx Virtex-E series field programmable gate array (FPGA). A highlight of the Virtex series is its configurable I/Os that can interface to a wide range of different logic types including low-voltage

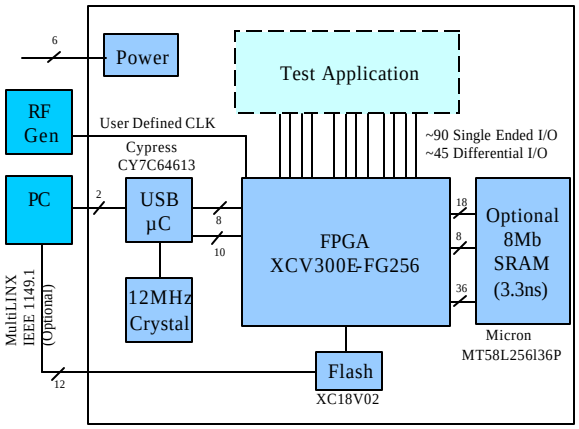

Figure 1. Digital Test Core Block Diagram.

differential PECL. In current designs, the specific chip used is an XCV300E in a 256-pin fine-pitch ball grid array package. The programmable nature of the chip allows test engineers to update and customize tests for future technologies. A computer is needed to provide test data and analyze results, but the critical testing logic is contained within the miniature tester. A Cypress microcontroller (Cypress CY7C64603) is used to process the USB signals and provide the data to and from the Xilinx FPGA. Current versions of the DTC use the USB 1.1 standard which operates at 12Mbps. Future versions of the DTC will use the USB 2.0 standard which operates at a rate of 480 Mbps.

The I/Os of the Virtex FPGA were verified to operate at speeds up to 622Mbps as specified by the manufacturer. Newer Virtex series FPGAs have I/O speeds up to 840Mbps. While these speeds are high enough to compete with currently available ATE, higher speeds are necessary for some devices.

Current versions of the DTC are coupled with external high-speed PECL logic, which times and formats the signals, distributes the clocks, and captures preprocesses incoming data. The PECL logic enables operation at higher speeds (~4.8Gbps). Future version will include SiGe devices to performs similar functions, but operate at much higher-speeds (~10Gbps).

The overall cost of the system depends on the number of channels needed and the test functions required for a specific application. Because the components of the digital test core are all off-the-shelve parts, the cost is generally small (on the order of hundreds of dollars), especially when compared with multi-million dollar ATE. The DTC can also replace standalone test equipment such bit error-rate testers, pattern generators, jitter measurement devices. While most of these standalone devices only provide a few channels, the DTC can provide hundreds, replacing many of these devices in a small package.

While the DTC was originally developed for ATE support, it has evolved so it is now ideally suited for standalone and embedded testing. Both configurations are shown in the next sections.

3. Opto-electronic Pattern Generator/Sampler

Optical testing is an order of magnitude more costly due to higher precision and operating frequencies. Traditionally, pattern generators produce signals to the transmitter, which performs the electrical to optical conversion. After the optical test, the receivers translate the signal back to bit-error rate testers. This application can benefit greatly from use of the digital test core by replacing this equipment.

In this specific application, the four-bit parallel output data is transmitted through coaxial connections to four different wavelength lasers, optically combined through wave-division multiplexing, and then transmitted over a single optical fiber. Incoming data from the fiber is demultiplexed to four-bit parallel electrical pulses, sampled by the PECL circuits, and transmitted to the DTC. A logic block diagram is shown in Figure 2. The optical component can also be removed, and the circuit can be used in a loop-back configuration, or as an electronic-only multi-gigahertz tester.

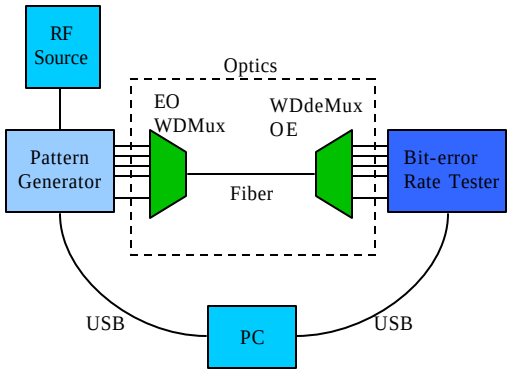

Figure 2. Opto-electronic interface overview.

Four-bit words are transmitted during each clock cycle along with a presence bit, which signals that the data is valid. A trigger bit is included for output to an oscilloscope for characterization of the board. Four digitally-programmable delay PECL chips set variable pulse widths and delays. The delay range is 10ns with a resolution of 10ps. The four-bit data words are synchronized, while the presence bit is offset to signal when the data is valid.

Four high-speed input channels are also provided with an input for a high-speed clock. The receiver channels are designed to operate either independently or in synchronous operation with the transmitter. The data is captured using a PECL register and returned to the DTC. The DTC can perform simple analysis on the data and then transmit the raw data back to the computer for further analysis. The block diagram for this circuit is shown in Figure 3.

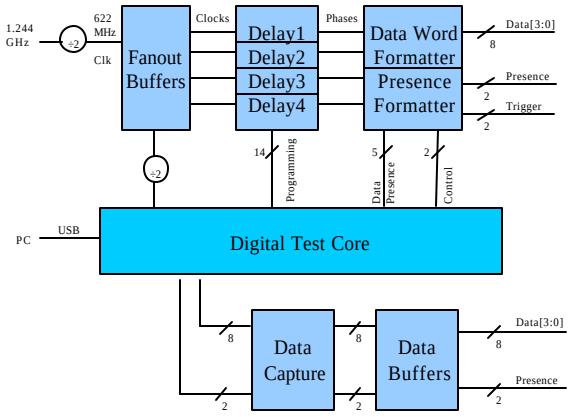

Figure 3. Opto-electronic Tx/Rx Block Diagram.

This opto-electronic transmitter and receiver was constructed as shown in Figure 4. The DTC was used without the optional SRAM since the on-chip memory in the Virtex FPGA was sufficient for this application. Separate power connections are included to isolate the relatively-noisy CMOS and the high-speed PECL logic. A socket for a PROM was also implemented for automatic programming of the FPGA upon board power-up.

The internal programming of the FPGA was designed to operate in different modes as needed by the user. In one of the modes, a series of four-bit words is entered in the computer and transmitted to DTC. Once the DTC has received the full sequence of test vectors, they are transmitted through the optics at-speed and then received to be stored on the chip. The data is then returned to the user for analysis. In another mode, the DTC transmits a free-running pseudo-random sequence of 4-bit words, and compares them with the returned values. It then stores statistical data, such as number of errors over a given number of cycles. This data is then transmitted back to the user.

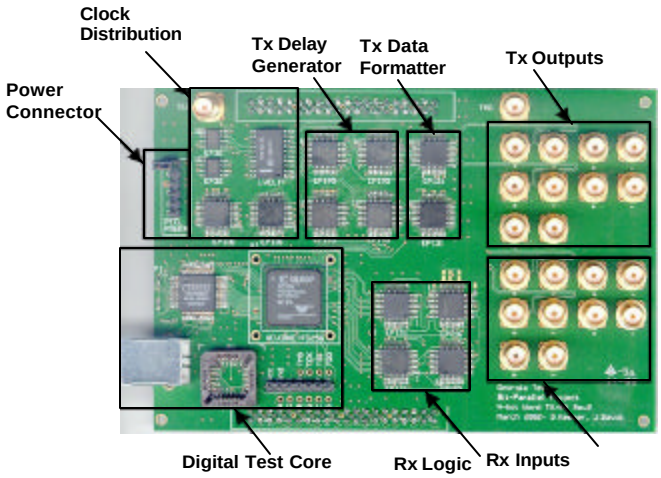

Figure 4. Multi-gigahertz Tx/Rx Photograph [2].

After construction of the miniature tester, an oscilloscope was used to measure the outputs of the four channels as shown in Figure 5. This sequence of words (1101,1011) was transmitted in the default return-to-zero fashion. The maximum pulse width of a high logic signal is half of the clock frequency. All four signals are source synchronous on board. Steps must be taken to maintain this off board, such as using matched length cables, since only one set of timing information is provided for all channels. One goal of the wave-division multiplexing scheme is to maintain this source synchronous behavior when returning the data to the DTC.

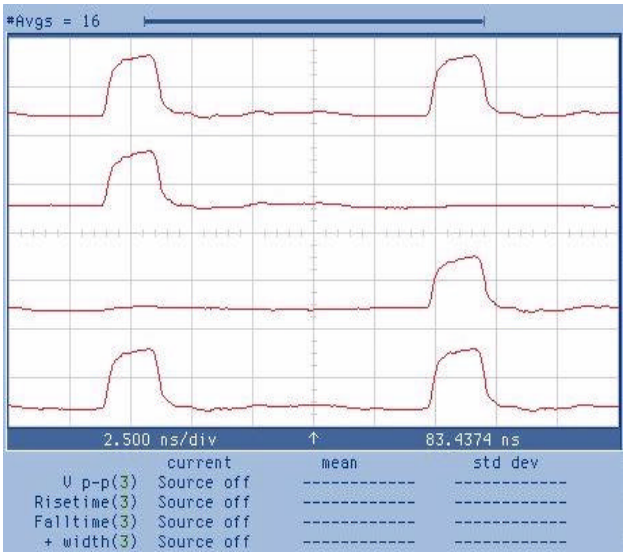

Figure 5. Opto-electronic Transmitter - Four Data Outputs

Even though the maximum data rate of the Virtex chips is 622Mbps, the pulse widths can be shortened by the PECL chips because of their faster rise and fall times. The measured rise and fall times are 150-200ps, which resulted in a minimum pulse width of about 300ps. This proves the

data rate of the PECL chips can exceed 3 Gbps per channel. This minimum pulse width is shown in Figure 6.

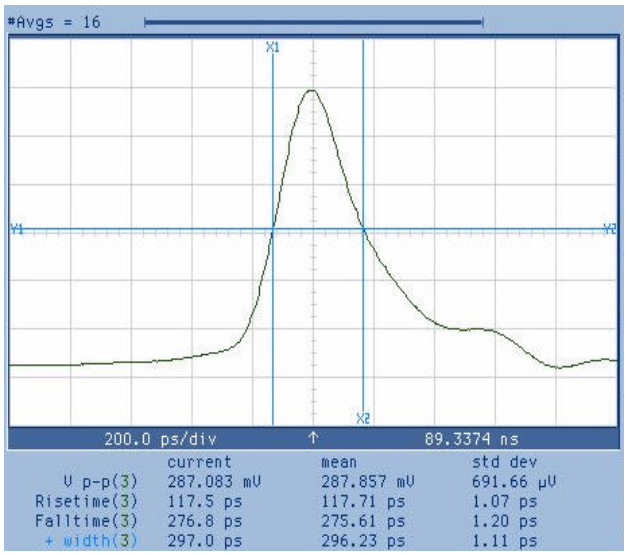

Figure 6. Opto-electronic Transmitter - Minimum Pulse Width

Equally important as short pulse width of the outputs is accurate edge placement. The more precisely the data outputs are placed relative to the presence output, the faster the circuit can operate. If the presence bit operates as a clock to a flip-flop, the setup-and-hold time is minimized with well-timed clock placement. The delay circuits on the board have a resolution of 10ps per step. This means pulse width can be measured with a resolution of 10ps. However, other factors such as jitter can affect the accuracy of the signals. Figure 7 shows the rising edge of the data output being changed in 20ps increments.

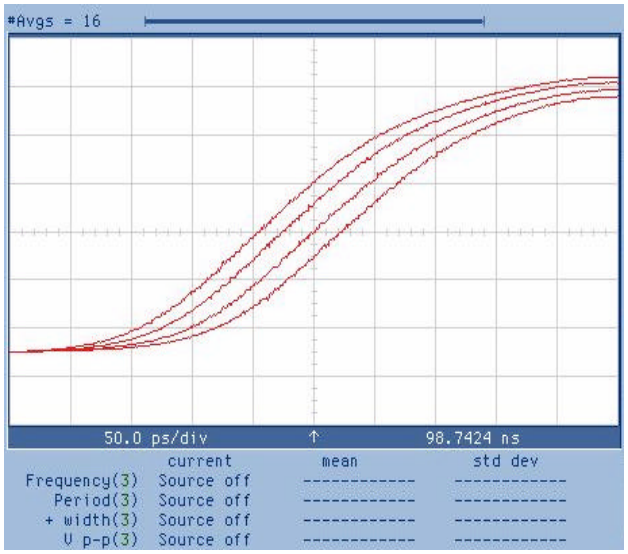

Figure 7. Opto-electronic Transmitter - 20ps Edge Placement Resolution

The delay circuits using their minimum step size of 10ps is shown in Figure 8. The delay chips are programmed with a 10-bit number for 10.24ns resolution. Each of the bits has a certain delay associated with it (10ps, 20ps, 40ps, 80ps, 160ps, etc.), and they add to obtain any offset within that range. However, each bit has a certain percent error associated with it. Even with a 1% error of each bit, the impact can be significant. The most significant bit has an offset of 5.12ns., 1% of which is 51ps. These offset errors can change the 10ps resolution and create a non-linearity in the delay programming as seen in Figure 8.

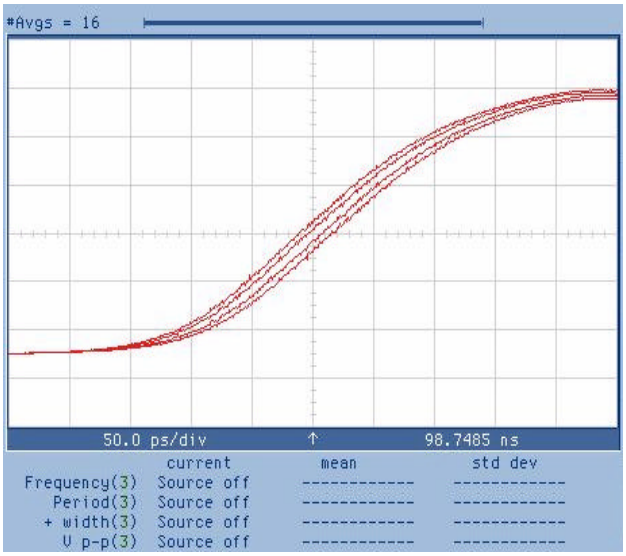

Figure 8. Opto-electronic Transmitter - 10ps Edge Placement Resolution

With edge rates of 150ps, error of even 1% is too high. However, the circuit is designed so that it can be calibrated to still obtain any delay by measuring the error on each bit of the delay chip. As long as the delays are linear over the whole range, the cumulative error can be computed for every delay value by simply adding the measured delay of each relevant bit. The calibrated delay timing is programmed into the software to automatically set the true delay by searching for the closest matching offset. For example, if one channel is set to 150ps, the true value is actually 179ps. By measuring the cumulative errors, setting the value to be 120ps produces a true value of 148ps, which is much closer to the 150ps desired. A section of the measured error is shown in Figure 9.

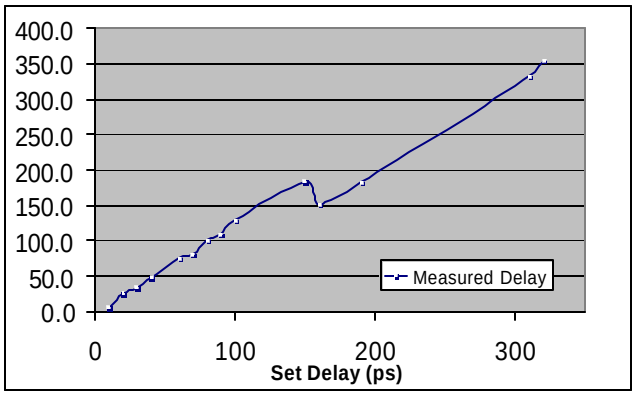

Figure 9. Delay Programming Uncalibrated Error

Even with the accuracy of the relative timing, the reliability of the signal is limited by the jitter. From the layout of the DTC, the main contribution of jitter comes from the input clock source. The statistics are shown in Figure 10. Currently the true measurement of jitter is limited by the RF clock source, but better equipment will be employed for the future.

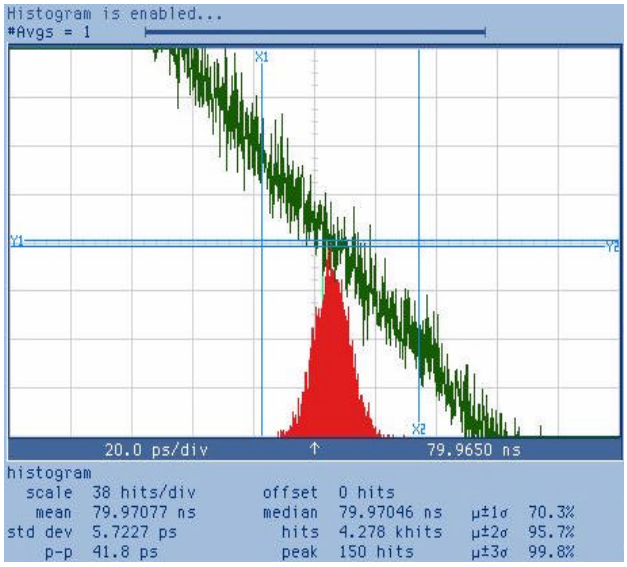

Figure 10. Opto-electronic Transmitter – Jitter Measurements

Once the timing information has been calibrated and programmed, the data is transmitted through the word formatters to the optical transceivers. The optical signal should track the electrical signals exactly in regards to timing. Due to optical requirements, an edge transition must occur within a certain time to maintain signal integrity. Currently, the user is required to ensure this requirement due to the full manual control of the data stream. Further development of software will remove this requirement if needed. The electrical to optical conversion is shown in Figure 11.

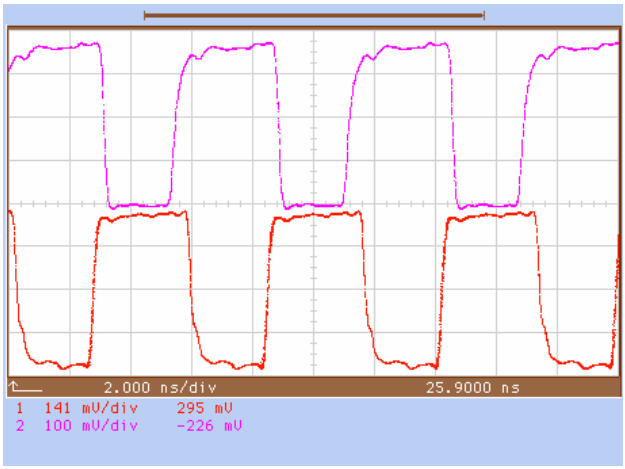

Figure 11. Electrical/Optical Conversion

Some issues remain, such as transmission line effects from connectors, cabling, and oscilloscope probes as can be seen in the Figure 6. The current physical setup is shown in Figure 12. With four data channels and a presence channel, all operating differentially, a total of 20 cables are used for the transmitter and receiver. This setup was originally planned to divide the optical components from the electrical components, since each was being developed by separate research teams. The next generation of this project will be a single board with all of the components integrated on it. This will not only simplify the physical aspect of connecting the two projects, but also minimize transmission line effects from the cabling.

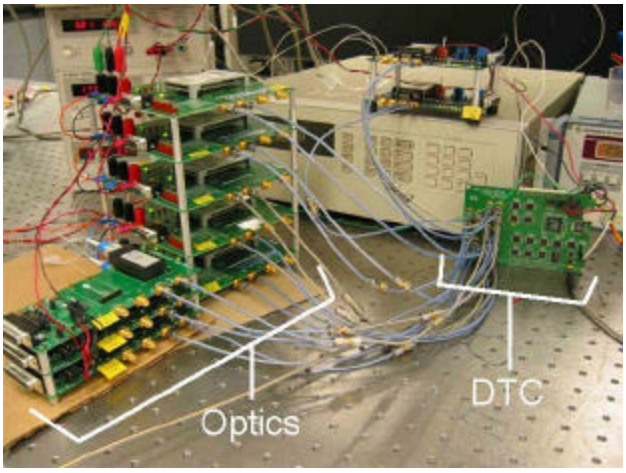

Figure 12. Opto-electronic Setup

The next generation of the optoelectronic tester is currently in the design stage. It will operate up to 10Gbps using new SiGe parts. As previously stated, all components will be integrated into one circuit board. The final goal of this project is to reach 128 digital channels combined using wave-division multiplexing into one fiber producing an aggregate data rate of 1.28 Terabits-per-

second over one optical channel. Since the DTC is designed to easily scale with regards to channel count, this is definitely an attainable goal.

4. Nano-scale Wafer-level Prober

The digital test core is also perfectly suited for near-autonomous testing of high-performance nano-scale wafer level packaged devices. The DTC is customized to specifically support the BIST features contained within a particular device. Such features include boundary scan, internal scan, internal pattern generators, and internal response analyzers. When these features are accessed using the IEEE 1149.x standards, only a very limited number of external pins are required. Furthermore, in most cases these few test pins do not operate at-speed, but at much lower frequencies. By supplementing these with timing reference signals, precise at-speed testing of both the internal logic and external interfaces is possible.

Most BIST strategies have a need for interface signals supporting standard test busses, and a need for precise timing reference signals. The application of such BIST strategies has become commonplace for system-on-chip (SOC) devices today. In large SOCs, major blocks of logic are often assembled from multiple design sources. When this is done, each design group provides test patterns and sequences for the subcircuits. These tests can be applied to the embedded logic blocks if the global SOC design is partitioned (usually with a scan-design approach). The individual tests can be initiated with standard commands through the IEEE 1149.x standard test busses. This approach is becoming a defacto standard design-for-test (DFT) practice in large SOCs today. It is expected to be applied even more universally for nanoscale wafer-level packaged devices [2].

If the number of independent I/O signals needed for testing is minimized, then a much smaller-scale test system can be used (as compared with traditional ATE). Providing logic to support the IEEE1149.x standard is not difficult, and can be accomplished using equipment. However, if accurate high-speed tests are required, then at least one (and usually several) timing reference signal is also required. The generation and control of these multi-gigahertz signals is not trivial, but attainable using the DTC.

Figure 13 illustrates a test configuration for nano-scale wafer-level packaged devices. The setup is similar to conventional wafer-probing, but with the inclusion of the DTC. The packaged wafer is placed on a movable wafer "chuck". A particular die site is then positioned beneath an "interposer." One side of the interposer is designed to mechanically align the leads of the wafer-level package and to provide a temporary pressure-contact for all electrical signals, including power and ground pins. The other side is mounted to a conventional multilayer PCB which further distributes the signals to pins or connectors that mate to the DTC I/Os. Multiple DTCs can be used for parallel testing of many devices on a single wafer, greatly increasing the test throughput.

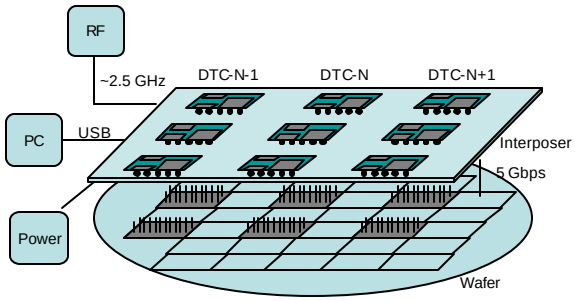

Figure 13. Parallel (array) testing using multiple DTCs.

All of the controls and global sequences of the various self-tests within the IC are administered automatically via the DTC. The tests are all setup by the user through the USB port. During operation, the various BIST sequences are applied within the IC, results are communicated back to the DTC, and a final test decision (pass or fail) is sent through the USB to a controlling computer. The wafer chuck is then repositioned to a new die site, and the process is repeated.

For nano-scale wafer-level packages the parallel expansion of the probe setup may be limited by the total force necessary to achieve reliable contact to ten/ hundreds of thousands of device leads. Part of the process design development for nano-scale leads therefore includes limitations on the force per-lead required for reliable pressure contact.

The high-speed timing signals needed for the test have been proven in the previous section to be easily provided by the DTC. In order to increase the data rate, a slightly different approach is used. Many low-speeds signals (622Mbps) are serialized into two half-speed signal (~2.5Gbps). These two signals are precisely timed and input to a precision XOR gate producing one high-speed signal (~5.0Gbps). The returning data is captured and stored in the DTC. The block diagram is shown in Figure 14.

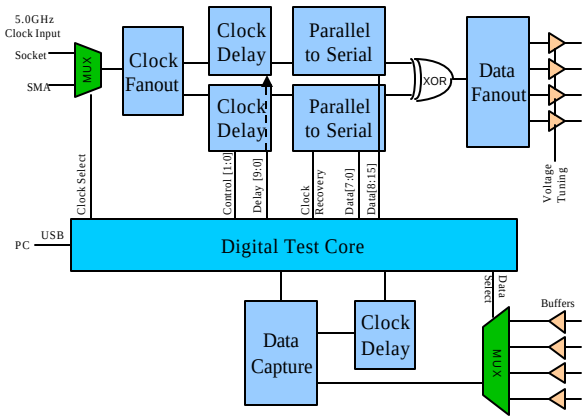

Figure 14. Nano-scale wafer-prober - Block Diagram

The prototype circuit has been partially constructed as shown in Figure 15. The clock signal can be input through the SMA connector, or through the test socket connectors. All test signals are also transmitted through these connectors to a motherboard which will have the capability of mounting multiple DTCs. The USB and power will be routed through the connectors as well to minimize the cabling when attached to the motherboard, but can also be directly connected to the DTC during development. The clock distribution, timing generation, data multiplexing, and I/O buffering is all handled in the support logic chips surrounding the DTC. The prototype board supports four high-speed differential I/Os.

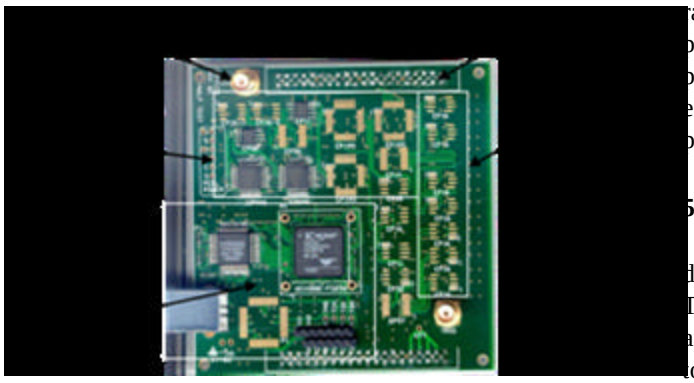

Figure 15. Nano-scale Wafer-prober Photograph

In preliminary testing, the signal of one half-speed (~2.5Gbps) signal of the prototype board was measured as shown in Figure 14. The input clock is set to 2.2GHz, and a 1010 pattern is configured by the digital test core. Given the preliminary nature of the data, the 2.5Gbps rate should be attainable for the half-speed signal. The high-speed signal is a direct XOR of the two half-speed signals, and with precise timing programming, data rates upwards of 5.0Gbps will be produced.

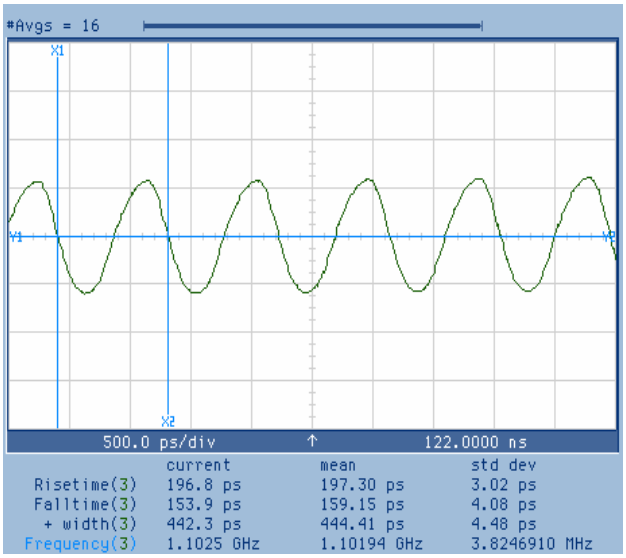

Figure 16. Nano-scale Wafer-prober – Half-speed Signal Output (2.2Gbps)

Since the DTC is easily scalable, multiple I/Os can be produced using similar techniques. The highest pin density of current programmable logic devices is roughly 2,000 I/Os, each operating at 622Mbps. With the serializing/multiplexing techniques previously described, this can amount to hundreds of multi-gigabit I/Os per DTC. If more I/Os are needed, then multiple instances of the DTC can be used.

As newer technologies develop, such as SiGe, data rates can exceed 10Gbps using similar techniques. With projected rise and fall times of 40ps, coupled with edge placement resolution of less than 10ps, the DTC can be easily upgraded to test the next generation of wafer level packaged circuits.

5. Conclusions

In this paper we have presented validation of the digital test core as a standalone and embedded tester. The DTC provides a robust interface in multiple testing applications, from a standalone opto-electronic test bed, to an embedded wafer-level prober providing an interface to BIST structures in the IC. The DTC also provides programmable precision timing references for at-speed test and characterization of wafer-level packaged ICs. The overall effect of the DTC combines the general use of ATE, without the high cost; and the test simplification of BIST, but without the complexity of silicon integration.

Acknowledgments

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