36-Node Data Vortex Implementation

0.0 Introduction (BAS)
This document details the design specifications for the first ever implementation of a complete Dava Vortex optical switching fabric. An introduction to the Data Vortex optical interconnection network topology can be found in the literature [Yang 2000, Yang 2001]. Moreover, previously published works [Yang 2002, Lu 2003, Lu 2004] have required the construction of small subsystems within a Data Vortex topology. Traffic patterns and signal integrity have been simulated extensively [Yang 2002, Small 2003], and the functionality of the Data Vortex node structure has been studied [Yang 2002, Lu 2003].

The primary design discussed implements a Data Vortex topology with the dimensions $A=3$, $H=4$, $C=3$, requiring 26 total switching nodes, and allowing for 12 input and 12 output ports. In addition to this basic structure, a larger system with $A=5$, $H=4$, and $C=3$ is mentioned since it permits 20 input and 20 output ports with 60 switching nodes. Many interesting applications require at least 16 computing elements, and the presented design is easily configured to this larger structure with minimal added complexity.

The physical implementation requires numerous subsystems. Each node of course has several optical components, and also requires an electronic control circuit, interfaced by optoelectronic and electrooptic components. In designing all of these interconnected subsystems, numerous features must be considered, all of which are interdependent. Even the physical structure and packaging for such a complicated system must be carefully arranged. Moreover, entire systems are required in order to implement the correct input and output port structure.

1.0 System Overview (BAS)
The envisioned Data Vortex implementation will contain 36 internal switching nodes, resulting in a port count of $12 \times 12$. The design is easily expandable to 60 nodes, arranged in a $20 \times 20$ switching configuration. The 36-node design utilizes 3 angle dimensions, with 3 cylinders, each with a height of 4 (see Fig. 1a); the 60-node system requires 5 angles (Fig. 1b). In addition to the optical and electronic switching nodes, a total of 60 (100 for the 60-node implementation) fiber links and 24 (40) inter-node electronic control cables are necessary.

![Figure 1. Topological graphs of the 12×12 and 20×20 Data Vortex systems to be implemented.](image)
The switching nodes are indeed the most important and most complex elements of this switching system. Each node requires two semiconductor optical amplifiers (SOAs), a few passive optical components, two photodetectors, and a myriad of high-speed electronics and optoelectronics circuitry. The passive optical have been packaged together by the vendor and so will be considered a blackbox throughout the remained of this whitepaper; the technology is very straightforward and extraordinarily robust.

1.1 Optics (BAS)
There are two important aspects of the optical system that must function correctly in order for the switching architecture to behave well: power and delay. The optical components of the nodes must therefore be specified with both of these considerations in mind, although variance can be tolerated since the system as a whole is quite robust and adjustable.

Furthermore, in order to utilize the potential bandwidth of this switching fabric, the system should utilize as much of the C-band (1528.77 nm to 1577.03 nm). The components selected do indeed operate almost uniformly over the range C17–C58 (1531.12–1563.46 nm), with a variance of only about 1.5 dB. Fig 2 depicts a typical gain profile for a Kamelian SOA. The effects of saturation are more pronounced at high signal power levels, and ASE (amplified spontaneous emission) noise at lower levels. Therefore, SOAs have an optimal input power at which the signal distortion is minimal (also Fig. 2).
As each pack traverses the nodes, it loses 30% of its power to the photodetectors and only another 50% remains on each branch (east or south) due to this necessary coupling. The SOA then boosts the power by about 5 dB, just enough to compensate for these coupling losses as well as the inherent connection losses and other efficiencies throughout the fiberoptic node; the SOA also introduces a small amount of noise. In order to minimize the noise generated by the SOA, the power level should be adjusted so that the amplifier is within its linear operating regime. Fig. 3 depicts the total power level of an optical packet and as it passes through the various optical components. In order to stay within the bounds of the linear operating regime for as many node hops as possible, packets should be launched with a total of -14 dBm of average optical power. But it can be seen that the tolerance is quite reasonable; imbalances in the gains and losses are acceptable while maintaining signal power that remains within the linear regime.

The delay of the optical pathways must be set so that the header and frame information have enough time to be processed before the packet reaches the switching element. The details of the system timing are discussed in more detail below.
1.2 Optoelectronics (OLL)
The optical receiver consists of a PIN diode and a trans-impedance amplifier (TIA) followed by a limiting amplifier. A +3.3V PIN-TIA module was selected from Appointech, which uses an InGaAs PIN photodiode and a CMOS trans-impedance amplifier from Mindspeed, integrated inside a hermetically sealed TO-46 can (sketched in Fig. 4, pinout Table 1). The module has a bandwidth of 115 MHz with a sensitivity of -22 dBm. This particular module was selected because it was designed with no internal AC coupling, allowing bursty data to be processed. It also offers differential output, which interfaces well with the differential input of the limiting amplifier.

![Figure 4: Schematic of PIN-TIA module.](image)

Table 1: PIN-TIA Module Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>Power-supply ground</td>
</tr>
<tr>
<td>2</td>
<td>Dout</td>
<td>Data out, connect to MAX3645 DIN+ through a series resistor</td>
</tr>
<tr>
<td>3</td>
<td>Dout_bar</td>
<td>Data bar out, connect to MAX3645 DIN- through a series resistor</td>
</tr>
<tr>
<td>4</td>
<td>Vcc</td>
<td>Power-supply 3.3 V</td>
</tr>
</tbody>
</table>

The CMOS TIA will convert the photocurrent to voltage with a high differential gain of 200 kΩ at low signal levels. The differential output voltage is 800 mV and is designed to drive a load greater than 500 Ω. The 2 ns rise and fall times allow the processing of digital signals rates up to 155 Mbps (Fig. 5).

Following the PIN-TIA module is the MAX3645 limiting amplifier with 2 mV peak-to-peak input sensitivity and PECL data outputs; it requires standard termination, which is ideal for interfacing with the logic gates. It can amplify data at rates from 125 Mbps to 200 Mbps (packet lengths from 5 ns to 8 ns). The +3.0 V to +5.5 V MAX3645 is available in 16-pin QSOP packages.

The common mode output voltage of the TIA is Vcc/2 (1.65 V). It should match the common mode input voltage of the limiting amplifier using a resistive network. The data input pins are internally DC biased at approximately 4 V via the Rin resistors. The Limiting amplifier should be DC coupled or, if it is AC coupled, capacitors must be large enough to pass the lowest input frequencies (consecutive ‘1’s or ‘0’s) of interest. For example, setting the capacitors to 10nF will give a typical 3-dB bandwidth of approximately 3.5 kHz.

The limiting amplifier (LA, pinout Table 2) includes an auto-zero circuit. In the absence of data, the feedback amplifier and summing circuit cancel the inherent offset voltage of the signal path, keeping the comparator at its toggle point. The offset loop might lead to malfunction, i.e. the input offset is larger than the input signal coming from the TIA device. To match the common mode voltage between the TIA and the LA devices, a resistive network can be used, or

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the power supply for the LA can be shifted relative to the TIA power supply. Another solution is to disable the offset loop by shorting the CZP and CZN pins or to compensate any differential input offset of the LA by applying a differential voltage to CZP and CZN.

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CAZ2</td>
<td>Offset-correction loop. Short CAZ1 and CAZ2 to disable</td>
</tr>
<tr>
<td>2</td>
<td>CAZ1</td>
<td>Offset-correction loop. Short CAZ1 and CAZ2 to disable</td>
</tr>
<tr>
<td>3</td>
<td>GNDA</td>
<td>Analog Supply Ground. Same potential as the GNDE pin.</td>
</tr>
<tr>
<td>4</td>
<td>DIN+</td>
<td>Positive data input. Connected to PIN-TIA module Dout</td>
</tr>
<tr>
<td>5</td>
<td>DIN-</td>
<td>Negative data input. Connected to PIN-TIA module DoutN</td>
</tr>
<tr>
<td>6</td>
<td>VCCA</td>
<td>+2.97 V to +5.5 V Supply. Same potential as the VCCE pin.</td>
</tr>
<tr>
<td>7</td>
<td>CSD</td>
<td>Connect the CSD capacitor to VCCA</td>
</tr>
<tr>
<td>8</td>
<td>DIS</td>
<td>Disable input. High enabled.</td>
</tr>
<tr>
<td>9</td>
<td>LOS</td>
<td>Loss-of-signal output. Low when signal level is above threshold.</td>
</tr>
<tr>
<td>10</td>
<td>LOSB</td>
<td>Loss-of-signal output. High when signal level is above threshold.</td>
</tr>
<tr>
<td>11</td>
<td>CNDE</td>
<td>Digital Supply Ground. Same potential as GNDA pin.</td>
</tr>
<tr>
<td>12</td>
<td>DOUT-</td>
<td>Negative data output, PECL. Connect to logic gate.</td>
</tr>
<tr>
<td>13</td>
<td>DOUT+</td>
<td>Positive data output, PECL. Connect to logic gate.</td>
</tr>
<tr>
<td>14</td>
<td>VCCE</td>
<td>+2.97 V to +5.5 V Supply. Same potential as the VCCA pin.</td>
</tr>
<tr>
<td>15</td>
<td>N.C.</td>
<td>No connection</td>
</tr>
<tr>
<td>16</td>
<td>TH</td>
<td>Resistor to ground sets the LOS threshold.</td>
</tr>
</tbody>
</table>

1.3 Electronics (AS)
Each node’s routing decision is processed electronically. After the frame and the correct header channels have been optically filtered, they undergo an optical-to-electrical conversion. These two inputs and a control electronic signal received from a previous node, along with internal setup jumpers, determine the destination of a packet (south or east), and turn on a current driver that enables the corresponding SOA.

The logic is implemented with one of the fastest electronic logic families commercially available, low-voltage positive-referenced emitter coupled logic (LVPECL). These electronic logic gates can operate at up to 3 Gbps. Improvements in the electronic speed of the optical
components are currently being investigated, so that a Data Vortex system could operate with packet frequencies at this electronically limited rate.

1.3.1 Digital circuitry
Input optical packets are routed either to the inner node (via south) or to the next node of the same cylinder (via east). A simple algorithm has been developed to processes this decision: two signals, normally the frame and one of the headers, are compared to the preset state of two jumpers. Generally, the frame jumper is set to high and the header jumper is set based upon its location in the Data Vortex topology. Otherwise, these jumpers are reconfigured to resolve a 2-bit (or 3-bit for the 20×20 implementation) angular address coding in the innermost cylinder. A schematic of this logic is presented as Fig. 6.

The decision rule is as follows:

\[
\text{If } \begin{cases} \text{(Frame == Frame-jumper)} \text{ and } \text{(Header == Header-jumper)} \end{cases} \\
\text{If (Cin is high)} \\
\text{Route South} \\
\text{Else} \\
\text{Route East} \\
\text{Else If (Frame == 1) or (Header == 1)} \\
\text{Route East} \\
\text{Else} \\
\text{Don’t Route.}
\]

Whenever routing east, the enable output signal should be low, otherwise high.

![Routing Node Logic Diagram](image)

**Figure 6: Routing Node Logic**

In addition to this simple logical function, the digital electronic circuitry also includes several debugging features. The south and east enable signals can be read from SMB microwave cable connectors, and LEDs echo all of the relevant signals. Moreover, two variable-latency devices were added to the design, one on each output path. The latency range of each of these components is from 2.2 ns to 12 ns, with 20 ps resolution; the exact value is controlled by a DIP-switch array. This design allows for timing compensation for latency variations in the board traces lengths, in the optical fibers lengths, and in the passive optical components assembly. The default setting of each variable latency device will probably be about 4 ns.

The speed requirements of the circuit necessitate the use of high-speed logic gates and interconnection components. Differential signals and LVPECL standard high-speed logic (PECL
@ 3.3V) gates were selected to meet the high-speed requirements. The devices will be purchased from ON Semiconductor, the market leader in ECL and PECL devices.

Signal integrity issues dictate careful design and layout of the printed circuit board with regard to signal routing, termination, layering, etc. The board is designed to handle a maximum frequency of 2 GHz (minimum packet duration of 500 ps). It is manufactured with standard PCB technology: a 4-layer board, standard spacing, width and heights, with FR-4 traces. All electronic off-board high-speed connections use SMA-type connectors. (The schematics of the board are attached as Appendix A.)

The LEDs for visual traffic indication are connected to TTL monostable multi-vibrators to broaden the pulses from the nanosecond range to the millisecond range, which better suits the human eye.

Note that faster technologies in integrated circuits and in printed circuit board manufacturing are commercially available. ON Semiconductor, for example, offers silicon-germanium gates with a 33% faster propagation delay, and the utilization of new PCB printing technologies and materials can reduce the trace delay significantly. Optimized for low latency, the latency of the electronic logic, including the O/E conversion and the SOA switching time can be reduced to the around 5 ns. The SiGe ICs cost four times as much as the ICs used in this implementation, and advanced PCB technologies also bear additional costs. These performance improvements could easily be realized in future implementations, as long they are supported with appropriate funding.

1.3.2 SOA drive circuitry (OLL)
The current transmitter design approach uses a laser driver from Maxim Integrated Products (MAX3656ETG) that operates at data rates from 155 Mbps up to 2.5 Gbps with maximum rise and fall times of 85 ps. The laser driver provides current to the SOA to either enable (open) or disable (close) the routing of the optical packet to the south node (progression to the inner node) or east node (deflection to a node on the same cylinder). The laser driver accepts LVPECL, which makes it easy to interface with the logic gates. In this Data Vortex system implementation, only the generated modulation current is needed to drive the SOA. This particular device was selected for its physically small package and its low power consumption. The MAX3656 is packaged in a small 24-pin 4 mm × 4 mm thin QFN package (Figure 7) and typically consumes only 132 mW.

![Figure 7: MAX3656 pin configuration](image)
The driver selection was also based on the modulation current range; this driver can provide from 1 to 85 mA to the SOA. This current range allows up to 10 dB of gain from a typical Kamelian SOA. The amount of gain in each node is set \textit{a priori} during the construction of the system to compensate for the internal node loss as well as the fiber attenuation. Initial experimental measurements suggest a current setting of about 40 mA in order to compensate for these losses completely. Table A describes the pin connection setup for best interfacing with the SOA.

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 4, 9, 15, 18, 21</td>
<td>Vcc</td>
<td>Power supply voltage. Connect to 3.3 V.</td>
</tr>
<tr>
<td>2</td>
<td>IN +</td>
<td>Noninverting data input with on-chip biasing. Connect to noninverting data output of last logic stage. PECL levels</td>
</tr>
<tr>
<td>3</td>
<td>IN -</td>
<td>Inverting data input with on-chip biasing. Connect to inverting data output of last logic stage. PECL levels</td>
</tr>
<tr>
<td>5, 6</td>
<td>BEN+, BEN-</td>
<td>Not applicable for this implementation. Connect for PECL levels signal for testability.</td>
</tr>
<tr>
<td>7</td>
<td>EN_BAR</td>
<td>Enable input. Low for normal operation; float to disable modulation currents. Connect to ground and Vcc through jumper.</td>
</tr>
<tr>
<td>8, 11, 19</td>
<td>GND</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>10</td>
<td>FAIL_BAR</td>
<td>Not applicable for this implementation. Leave unconnected.</td>
</tr>
<tr>
<td>12</td>
<td>LONGB</td>
<td>Not applicable for this implementation. Connect to ground and Vcc through jumpers.</td>
</tr>
<tr>
<td>13, 14</td>
<td>BIAS-, BIAS+</td>
<td>Not applicable for this implementation. Connect through 15 Ω to Vcc.</td>
</tr>
<tr>
<td>16</td>
<td>OUT +</td>
<td>Noninverting laser modulation current output. Connect through series resistor to SOA anode (+).</td>
</tr>
<tr>
<td>17</td>
<td>OUT -</td>
<td>Inverting laser modulation current output. Connect through 15 Ω to Vcc.</td>
</tr>
<tr>
<td>20</td>
<td>MD</td>
<td>Not applicable for this implementation. Leave unconnected.</td>
</tr>
<tr>
<td>22</td>
<td>BIASMAX</td>
<td>Not applicable for this implementation. Connect through resistor to ground.</td>
</tr>
<tr>
<td>23</td>
<td>MODSET</td>
<td>Modulation current set. A resistor connected from this pin to ground sets the desired modulation current.</td>
</tr>
<tr>
<td>24</td>
<td>APCSET</td>
<td>Not applicable for this implementation. Connect through resistor to ground.</td>
</tr>
<tr>
<td>EP</td>
<td>Exposed Pad</td>
<td>Ground. This pad must be soldered to ground.</td>
</tr>
</tbody>
</table>

The modulation output stage is composed of differential pairs with programmable current sources. The circuit design is optimized for high-speed low-voltage (3.3V) DC-coupled operation; the modulation output is optimized for driving a 15 Ω load. The modulation current can swing up to 85 mA for data rates less than or equal to 1.25 Gbps. To minimize optical
output aberrations caused by signal reflection at the electrical interface to the SOA, a damping resistor is required for impedance matching. The combined resistance due to the series damping resistor and the equivalent series resistance of the SOA should be equal to 15 \( \Omega \). The modulation current is determined by the amount of gain the SOA should exhibit. The graph in Fig. 8 can be used to select the value of the resistor connected to pin MODSET. For a current setting of 40 mA, a 7 k\( \Omega \) resistor is required.

![Figure 8: Modulation current versus resistance value.](image)

1.4 Timing Analysis (AS, BAS)

The complex timing considerations for the nodes of this and any Data Vortex implementation require an understanding of the flow of data necessary to maintain synchronous operation within the system. Optical data enters each node at the optical coupler “blackbox;” one branch of optical data is then immediately routed to the optoelectronic systems and thence to the control electronics, while the other branch must be delayed over the duration of the electronic conversions and control logic decision. This first fundamental timing equality can be expressed algebraically as

\[
T_{dp} = T_1 + T_2 + T_3,
\]

with the optical branch delay \( T_{dp} \), optoelectronic conversion time \( T_1 \) (which also contains a small amount of logic), electronic decision logic delay \( T_2 \), and electrooptic (SOA) drive time \( T_3 \).
The second timing consideration is quite a bit more difficult: for correct synchronous operation of the control mechanism between cylinders, ingressing packets must have enough time to signal up to a deflecting packet and initiate the “block”. (This issue has been discussed extensively in the published Data Vortex literature.) Due to the intelligent design of the electronics, the control signal is required only during timing duration $T_2$; therefore, the path of the control signal is exactly equal to the delay of the necessary logic and that of the microwave cable: $T_2 + T_C$. Moreover, the data must travel through the entire node and over either a deflection fiber or an ingression (progression) fiber. These requirements lead to the second fundamental timing equality:

$$T_0 + T_1 + T_2 + T_3 + T_D = T_0 + T_1 + T_2 + T_C + T_2 + T_3 + T_P$$

$$T_D - T_P = T_2 + T_C.$$

Moreover, the timing block $T_2$ contains a tunable delay element, allowing its total delay to range from 3.2 to 13.0 ns. Using the values given in Fig. 9, the above fundamental timing equalities work out to be

$$T_{dp} = T_1 + T_2 + T_3$$

$$6.1 \text{ ns} \leq T_{dp} \leq 15.9 \text{ ns};$$

and

$$T_D - T_P = T_2 + T_C$$

$$3.8 \text{ ns} \leq T_D - T_P \leq 13.6 \text{ ns}.$$

The length of the optical delay path can therefore be set to 5.9 ns (about 120 cm), and the difference between the deflection path and the progression path lengths can be set to 4.9 ns (about 100 cm). The tunable delay element should therefore be set at 4.3 ns, requiring at least a 0.7-ns guard-time to ensure that the SOA is completely on before the data enters. Conventional guard-times from past experiments have been as long as 6 ns, so 0.7 ns is actually very short. At a payload clock rate of 10 GHz, this delay is equivalent to just 7 time-division bits at the beginning and at the end of the packet. In order to maintain a conservatively stable system, a guard-time of 1.0 ns will probably be used.
1.5 Physical Layout (JPM)

An individual node is arranged three-dimensionally, as shown in Fig. 10. The optoelectronics, electronic devices, and SOAs are arranged on a printed circuit board (PCB), which also has layers dedicated for power distribution and grounding. The back face of the board is adorned with LEDs and other debugging tools. The optical “blackbox” is arranged perpendicular to the circuit board, which allows for easy stacking, as described below.

Figure 10. Physical layout of printed circuit board and optical components for each node.

The 12×12 and 20×20 Data Vortex systems are configured cylindrically, where nodes are separated into groups of six based on the control lines that interconnect between these nodes (Fig. 11); all nodes within a group have the same angle value, so control lines must interconnect only within these groups of six. Each group has two subgroups of three nodes. The three nodes of the subgroup are placed next to each other in a vertical fashion, where one subgroup contains the top three nodes and the other subgroup contains the bottom three nodes.

This arrangement not only makes it easy to expand to systems with larger port-counts (e.g., from 12×12 to 20×20), but it also allows the control lines to be connected with the minimum possible latency. The figure on the right shows the expansion of boards into six vertically connected boards that make up a group in the implementation of the data vortex.

Figure 11. A topological depiction of the six nodes integrated into the circuit board.
Fig. 12 depicts the node stacking arrangement: each tower is 19” tall, and the diameter of the hexagon is approximately 12”. This configuration requires the optical interconnects to cross only the inner region of the hexagon, minimizing path latency and, hopefully, physical clutter.

The fibers must then be connected by the pattern illustrated in Fig. 13 in order to form the correct Data Vortex topology. A connection scheme was chosen where the outputs of the vortex are on the top and bottom of the boards while the inputs are in the middle of the boards. The other connections are for the internal nodes which act as routers only.

![Figure 12. Physical arrangement of nodes for a 12×12 Data Vortex: the 36 nodes are stacked in groups of six.](image)

![Figure 13. Diagram of the connection scheme for the 12×12 Data Vortex implementation. Progression fibers are black while deflection fibers are green; input nodes are shown in green, and output nodes in blue.](image)

1.6 Support Systems (JPM)

Another issue that must be analyzed is that of power consumption in the Data Vortex system. SOAs, receivers, and high-speed electronics certainly consume large amounts of power in a system of this size. However, the complexity of this problem has been minimized by the choice of voltages used for all components: only the standard voltages 3.3 V and 5 V are required. These voltages can easily be adjusted by using of high current voltage regulators. While a 36-node system will draw around 180 W, power supplies are readily available at these voltages and
at high current levels. Fortunately, the cost of powering a large-scale network will not be too significant. The current itself will be delivered through the large six-node circuit boards since they contain layers dedicated to power distribution.

Temperature control is a subsequent issue that should be addressed in a system that contains high speed devices. The SOAs and high-speed electronics may be subject to temperature changes from fast clock cycles and switching. High or inconstant temperatures affect how these devices perform. When the data vortex is at full capacity for long periods of time, these devices will be more prone to this problem. Previously, we used high power current drivers for the SOA’s which exhibited overheating and failure. The current design, however, dissipates significantly less power, and trials have indicated that temperature control is not necessary.

2.0 Interfacing Overview

It is important not to ignore the issues relating to the input and output of data to and from the switching fabric system. These necessary subsystems must be considered quite carefully since they are the only means of empirically verifying the functionality of the system.

2.1 Input Optics (OLL)

The Data Vortex network system requires an extinction ratio of at least 13 dB for a 10 Gbps NRZ payload. External amplitude modulation of a continuous-wave (CW) laser signal is the best commercial solution available today. The optical modulator also has the advantage of being DC-coupled allowing burst data transmission. This approach necessitates having the driver either on the interface board or selecting an integrated solution such like the Corning IM-4 product, which has a driver integrated with an optical modulator. Fig. 14 illustrates both approaches with some suggestions for the optoelectronics components. References to those components’ data sheets are included in the appendix. Note that other appropriate commercial components might exist in addition to those proposed.

Figure 14: External modulator with driver on the interface board (left); external modulator with integrated driver (right).

The modulator integrated with the driver module has some advantages over the non-integrated version. For optical performance analysis only, the integrated module can be used
without the E/O interface board. The integration also simplifies the board design layout and improves the signal integrity.

The non-return-to-zero (NRZ) modulation format has been selected for the header, frame, and payload. Investigations are underway to analyze the advantages of other modulation formats, such as return-to-zero (RZ) or phase-shift keying (PSK) for the payload. The current node logic structure, however, requires that the header and frame signals be encoded with the NRZ format.

2.2 Output Detectors (OLL)

The Data Vortex is an optical packet switching network system. Packets are routed at each internal node based on the packets’ addresses and on the global network traffic. The optical receiver of the destination node converts the optical signal to an electrical signal whenever a packet arrives to its destination. When no packet is present, the optical receiver remains idle and ready to process the next packet. Because of packets arrive in bursts and not continuously, the receiver path needs to be DC-coupled to avoid the low-pass filtering any DC information.

Most commercial optoelectronics components are designed for the telecom market (e.g. SONET standard), which consists of a continuous flow of scrambled digital signals with no DC wander. This approach simplifies the integrated circuit design and requires AC-coupled signal paths between stages. The threshold circuit relies on a DC average of zero. If such an approach is used in burst-type communication, baseline wander occurs as shown in Fig. 15.

![Different coding schemes, with associated DC averages; baseline wander is from 0.](image)

Figure 15: Different coding schemes, with associated DC averages; baseline wander is from 0.

In a bursty mode system, the threshold decision circuit distorts the data pulse width, as the decision level between a logic ‘1’ and logic ‘0’ is no longer at 50% of the signal amplitude. Pulse width distortion between the optical and the electrical signal has been observed and is shown in Fig. 17.
To avoid the problem mentioned above, the optical receiver path should be designed with care to avoid the use of AC-coupling techniques. This can be done if the output common-mode voltage of the trans-impedance amplifier matches the input common-mode voltage of the post amplifier. A resistive network can be used, or the voltage supply of one of the two components can be changed with respect to the other, in order to match the signal levels. The data path is shown in Fig. 18, along with the part number of suggested commercial optoelectronic products.

Currently, the possibility of collaboration work in designing a burst-mode optical receiver is being considered with a few commercial vendors. There is certainly a strong demand for such a product in various applications.

Once the payload is converted to an electrical signal, it should be sampled to recover the data. Therefore, a clock is necessary to sample the data. The 10 Gbps packets are too short to have preamble bits for clock recovery. The other option would be to use a local clock. As long as the maximum burst length and frequency deviation can be limited, a variable data delay can be used to align the data to a fixed local clock. But the burden is now imposed on the integrated
circuit design. However, this approach is still being investigated, as are all-optical clock recovery techniques.

Because DWDM systems contain many optical channels, one channel could be used for a global clock, which would be routed along with a packet, as shown in Fig. 19. Using this approach, a synchronous clock would always be available at any node destination where a packet arrives. It is then sufficient to filter out the clock by taping some optical signals from the fiber as shown in Fig. 20. This design approach is strongly linked to what the next stage signal requirements are, and more work needs to be done to find the right components suiting this approach.

3.0 Experimental Overview
[How we’re going to run the PPGs and take BER and traffic pattern measurements.]

4.0 Future Improvements
The latency of the system can be substantially improved by utilizing integrated optical components. A single substrate could contain the necessary couplers and filters, and perhaps even the detectors and amplifiers. Then, employing state-of-the-art electronics would reduce the total node latency to around 1 ns.
Research is also currently underway to develop a gain-flattening filter for the SOAs. This would even out the gain experience by different wavelengths as they propagate through the system, thus making the WDM packets easier to manage and increasing the maximum hop count substantially.
5.0 References and Datasheets


Modulator driver


OKI KGL4126: [http://www.okioptical.com/ic_10g_optical_pack-ln.shtml](http://www.okioptical.com/ic_10g_optical_pack-ln.shtml)

Modulator, 10Gb/s, amplitude, photodiode:


Integrated modulator and driver module:


Photodetector and transimpedance amplifier:

Picometrix PT-12A: [http://www.picometrix.com/publicinfo.html](http://www.picometrix.com/publicinfo.html) (Registration required)

Multiplex MTRX192: [http://www.multiplexinc.com/content/pdf/summer/RX192DA_datasheet.pdf](http://www.multiplexinc.com/content/pdf/summer/RX192DA_datasheet.pdf)

Limiting or post amplifier: