

# Ultrahigh-Bandwidth Silicon Photonic Nanowire Waveguides for On-Chip Networks

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**Abstract**—An investigation of signal integrity in silicon photonic nanowire waveguides is performed for wavelength-division-multiplexed optical signals. First, we demonstrate the feasibility of ultrahigh-bandwidth integrated photonic networks by transmitting a 1.28-Tb/s data stream (32 wavelengths  $\times$  40-Gb/s) through a 5-cm-long silicon wire. Next, the crosstalk induced in the highly confined waveguide is evaluated, while varying the number of wavelength channels, with bit-error-rate measurements at 10 Gb/s per channel. The power penalty of a 24-channel signal is 3.3 dB, while the power penalty of a single-channel signal is 0.6 dB. Finally, single-channel power penalty measurements are taken over a wide range of input powers and indicate negligible change for launch powers of up to 7 dBm.

**Index Terms**—Multiprocessor interconnection, optical communication, optical crosstalk, optical waveguides, wavelength-division multiplexing (WDM).

## I. INTRODUCTION

RECENT advances in the density and complexity of photonic integrated circuits (PICs) have enabled the viable integration of complete optical systems on a monolithic semiconductor chip. As a result, PICs are envisioned as a plausible means of implementing on-chip and chip-to-chip interconnection networks [1], [2]. Because of the high modulation rates and wavelength parallelism made available by optical transmission and wavelength-division-multiplexing (WDM), the large bandwidth demands of high-performance computing

systems can be met with integrated optics. Further advantages can be realized by implementing such a system in the complementary metal-oxide-semiconductor (CMOS)-compatible silicon-on-insulator platform [3]. These benefits include ultra-compact footprint resulting from high index contrast, simple integration of electrical and optical components, and low-cost while at the same time extremely high-quality processing. Complex active and passive components have been envisioned and successfully fabricated in this material system [3]–[5]. An equally important consideration, however, is the performance of the interconnection medium: the waveguide or *photonic wire*. High-bandwidth WDM transmission schemes have been demonstrated in III–V materials without emphasizing the importance of the photonic waveguide, and without offering compatibility with the CMOS electronics platform [6], [7]. Here, we confirm that the low-loss silicon-wire-waveguide technology can be used both for on-chip networks and for chip-to-chip networks, where off-chip bandwidth is crucial.

In this letter, we investigate the suitability of silicon photonic wires for carrying ultrahigh-bandwidth WDM data streams. Our central result is to demonstrate the successful transmission of a 1.28-Tb/s stream through a 5-cm-long wire waveguide. The aggregate data rate, composed of 32 wavelengths, each modulated at 40-Gb/s, is the largest reported in a silicon photonic wire to date [8], [9]. Moreover, considering the area of conventional semiconductor dice (typically about 1 cm<sup>2</sup>), this length is sufficient to route a signal anywhere on the die, regardless of the network topology or routing scheme. Additionally, we evaluate the interchannel crosstalk induced by nonlinearities in the photonic wire with bit-error-rate (BER) measurements. These results, made possible by the recent improvements in the design and fabrication of the low-loss silicon wires, represent a significant step toward developing a complete toolbox for PIC design.

## II. EXPERIMENTAL SETUP AND WAVEGUIDE DEVICE

The experimental setup [Fig. 1(a)] for the BER measurements employs 24 continuous-wave communications lasers with outputs combined by a 32-channel multiplexer with 100-GHz channel spacing. The laser wavelengths are located on the ITU *C*-band, comprising channels C22–C32, C35–C38, and C43–C51. A LiNbO<sub>3</sub> modulator encodes a 2<sup>31</sup> – 1 pseudorandom bit sequence onto each lightwave at 10 Gb/s using the nonreturn-to-zero format. The signals are then decorrelated by 425 ps/nm using 25 km of single-mode fiber, which results in about 3.4 bits of delay between adjacent wavelengths. The light is coupled in and out of the chip through tapered fibers [Fig. 1(b)]. Following the silicon chip, the signal is amplified

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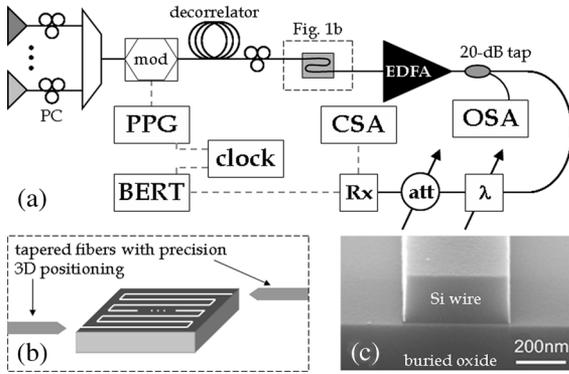


Fig. 1. (a) Diagram of the experimental setup, (b) schematic of the fiber coupling and wire waveguide layout, and (c) scanning electron microscope (SEM) image of the silicon photonic wire cross section.

by an erbium-doped fiber amplifier (EDFA), after which some of the power is tapped for monitoring on an optical spectrum analyzer (OSA). One wavelength channel is selected for measurement using a tunable filter, which is followed by an attenuator and a receiver module consisting of a p-i-n photodiode (PIN), transimpedance amplifier (TIA), and limiting amplifier (LA). The detected signal is evaluated with a communications signal analyzer (CSA) and a BER tester (BERT), which is synchronized directly to the pulse pattern generator (PPG) by a 10-GHz clock source. Polarization controllers (PCs) are used throughout.

The setup for the 1.28-Tb/s demonstration employs 32 channels, C21 (1560.61 nm) through C52 (1535.82 nm), each modulated at 40 Gb/s and decorrelated by 94 ps/nm in 5.5 km of fiber, resulting in about 3 bits of delay between adjacent wavelengths. In addition, a 40-Gb/s PIN-TIA replaces the former 10-Gb/s PIN-TIA-LA.

The silicon photonic wire is a single-mode waveguide with a height of 220 nm and a width of 520 nm [Fig. 1(c)]. The device was fabricated using the CMOS production line at the IBM T. J. Watson Research Center. Each end has an inverse-taper mode converter covered with index matching polymer, which allows efficient coupling ( $<1$  dB per facet) [10]. The 5-cm length was achieved by snaking the wire across the chip [Fig. 1(b)], making a total of 24  $90^\circ$ -bends with bending radii of  $6.5 \mu\text{m}$ . Dispersion and nonlinear parameters of the wire are similar to those shown in previous work [11]–[13].

### III. EXPERIMENTS AND RESULTS

First, we confirm the feasibility of ultrahigh-bandwidth networks utilizing silicon photonic wires by generating a 1.28-Tb/s data stream, composed of 32 40-Gb/s wavelength channels, and propagating the stream through the 5-cm wire. The input spectrum and a selection of eye diagrams before and after the waveguide propagation are shown (Fig. 2). A major source of degradation results from the amplification required to compensate the on-chip propagation loss ( $\sim 3$  dB/cm).

It should also be noted that the polarization states of the 32 channels, which are aligned prior to the multiplexer, drift slightly in the decorrelator by various amounts. Therefore, for the 40-Gb/s measurements only, the state of the PC preceding

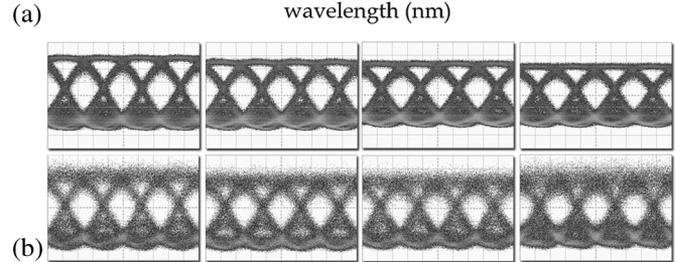
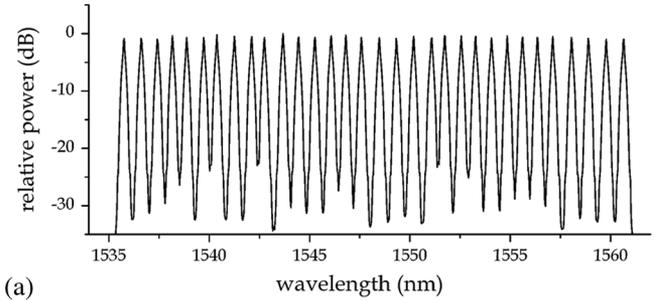


Fig. 2. (a) Input spectrum for the 1.28-Tb/s signal with a resolution bandwidth of 0.06 nm; (b) input (top) and output (bottom) eye diagrams for channels (from left to right) C23, C28, C46, and C51 with 10 ps/div.

the polarization-sensitive photonic wire was optimized for each channel while viewing the eye diagram. This drifting of the states of polarization across the wavelength channels, however, arises from the manner in which we simultaneously modulate the entire spectrum with a single modulator, and then decorrelate the channels to emulate 32 independent streams. In actual network implementations where independent data are encoded onto each channel separately before wavelength-multiplexing, this problem does not exist, because only a short length of fiber is required between the multiplexing and the fiber-to-chip coupling.

The second experiment characterizes the crosstalk between wavelength channels in the photonic wire with a peak launch power (i.e., “1” bit power) of approximately  $-6$  dBm per channel. The BER characteristics are evaluated at 10 Gb/s rather than 40 Gb/s, because a 40-Gb/s BERT was not available. Receiver sensitivity curves are taken before and after propagation through the 5-cm wire for a single probe wavelength, C36 (1548.51 nm). The observed power penalty is 0.6 dB (Fig. 3). Then, 20 additional wavelength channels are enabled and passed through the silicon wire alongside the probe, with the nearest channel being greater than 3 nm in wavelength from the probe. A degradation of 1.5 dB in the sensitivity curve at a BER of  $10^{-9}$  is noticed. Next, three more wavelengths are enabled, totaling 24 wavelength channels or 240 Gb/s. These wavelengths occupy *C*-band channels adjacent to the probe (C35, C37, and C38). The additional crosstalk from these channels further increases the power penalty by 1.1 dB. Finally, a sensitivity curve is taken for the 24-channel signal before entering the photonic wire. The resulting 24-channel power penalty is 3.3 dB. Given the length of the silicon photonic wire and the number of channels in the input signal, the measured penalty is quite tolerable. The reasonable overlap between the two extreme back-to-back curves (1-channel and 24-channels) in Fig. 3 indicates that the measured degradation is a result of crosstalk in the silicon wire, rather than crosstalk occurring elsewhere in the setup (e.g., the EDFA).

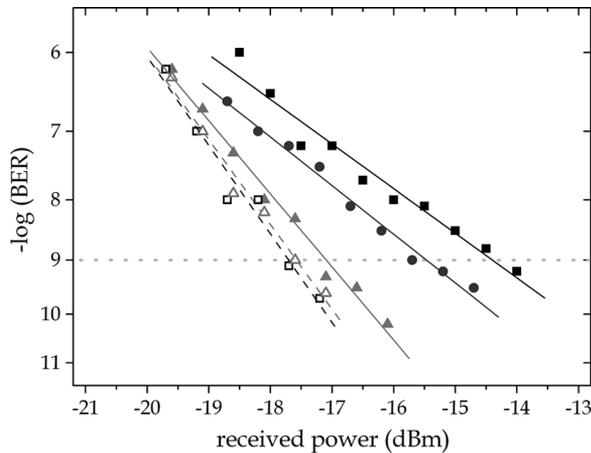


Fig. 3. BER curves at 10 Gb/s showing wavelength crosstalk in a 5-cm wire waveguide with symbols denoting single- ( $\blacktriangle$ ), 21- ( $\bullet$ ), and 24-channel ( $\blacksquare$ ) WDM signals. Measurements are taken for signals going through (solid lines, filled symbols) and bypassing (dashed lines, open symbols) the wire.

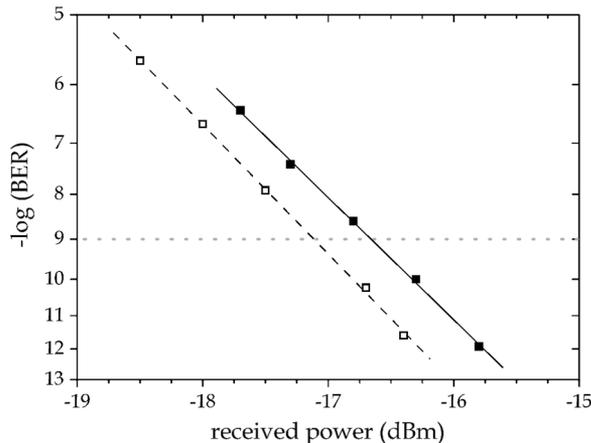


Fig. 4. BER curves at 10 Gb/s for a single wavelength channel injected into the 5-cm wire waveguide with more than 7 dBm of peak power. Measurements are taken for signals going through ( $\blacksquare$ ) and bypassing ( $\square$ ) the wire.

Previously, self-phase modulation (SPM) has been observed in silicon wires using picosecond pulses [12]. Typically, the injected powers required to observe SPM are a few tens of milliwatts with 0.4-cm-long wires. It is important to consider the power penalty induced when high-power signals are launched into much longer wires. Fig. 4 shows the BER curves for a single wavelength at 1550 nm with a peak (i.e., “1” bit) power of more than 7 dBm injected into the wire. The resulting 0.5-dB power penalty is within the experimental error of the previous single-channel measurement (0.6 dB, shown in Fig. 3), taken with a much lower launch power. (Of the seven BER curves shown in Figs. 3 and 4, the average of the root-mean-square (rms) errors for each curve is 0.1 dB with a maximum rms error of 0.2 dB.) This result confirms consistent power penalties over an input power dynamic range of more than 10 dB.

#### IV. CONCLUSION

We have successfully demonstrated the transport of terabit-per-second-scale WDM data signals using silicon photonic wires over sufficient distances for any on-chip network. An extensive investigation of the crosstalk is performed using 10-Gb/s channels. The interchannel nonlinear processes (e.g., cross-phase modulation and four-wave mixing) are more noticeable than intrachannel processes (e.g., SPM) for signals with many wavelengths. Yet even in a 5-cm-long dense WDM 10-Gb/s link, the wire exhibits only a 3.3-dB power penalty at a BER of  $10^{-9}$ . Finally, single-channel 10-Gb/s measurements with input powers ranging across approximately 13 dB, show no change in power penalty, indicating there could be enough power margin to meet at least a single-channel network’s optical power budget.

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