Wide Temperature Range Uncooled 2.5D Integrated Silicon Photonic DWDM Receiver

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***Abstract*—We demonstrate an eight channel DWDM 2.5D integrated microring receiver operating error-free at 16 Gbps per wavelength over 75 degrees Celsius range, while tracking fluctuations of 3.1 degrees Celsius per second, addressing the microring's sensitivity to challenging thermal environments in co-packaged optics in an eight wavelength package, achieving an aggregate bandwidth of 128 Gbps across the full temperature range.**

***Keywords*—silicon photonics, thermal control, optical receiver**

I. Introduction

To sustain the growth of computation systems, interconnect architectures increasingly rely on dense wavelength division multiplexing (DWDM) to provide the required bandwidth for next generation compute systems [1]. DWDM-based systems built using microring resonator (MRR) filters have the potential to be highly energy efficient and compact, in part due to the MRR's small footprint and wavelength selectivity [2]. A major challenge with MRRs implemented in Silicon Photonic (SiPh) platforms is their sensitivity to ambient temperature changes, requiring active thermal control to maintain the MRRs' 'lock' to their designated wavelength, as specified by the system architecture. To maximize energy efficiency and bandwidth, MRRs are integrated close to high power compute systems such as field-programmable gate arrays (FPGAs), graphics processing units (GPUs), or application specific integrated circuits (ASICs) [3]. The energy consumed by these devices, dissipated as highly localized heat, significantly increases ambient temperature experienced by the photonic integrated circuit (PIC), often in a highly localized manner, both spatially and temporally. This requires the MRRs to function over a wide temperature range. Prior work demonstrating the operational temperature range of MRRs only showed a single resonator [4] or a small operating range [5].

We present an eight channel receiver composed of a custom PIC with eight cascaded MRR filters, which is 2.5D integrated with two transimpedance amplifiers (TIAs) on an AlN interposer. The receiver operates error-free over a record 75 °C at 16 Gbps/channel with a bit error rate (BER) better than 10^{-12} and can maintain 25 Gbps/channel operation with a BER better than 10^{-9} over at least 65 °C. These give aggregate data rates of 128 and 200 Gbps respectively. This system is robust to both local compute-node induced heating, and external, environmental heating, and has multiple options for further expanding the operational thermal range.

II. Demonstration System

We demonstrate MRR filters operating over a wide temperature range using the system depicted in Fig. 1a. The core of our receiver is a custom PIC designed by our laboratory with eight cascaded MRR filters, each capable of filtering out a single optical wavelength and guiding it into a photodiode (PD). The MRRs have a full-width half-maximum (FWHM) of ∼70 GHz and free spectral range (FSR) of ∼26 nm [6]. Each MRR also has an integrated doped silicon heater to implement channel-specific thermal tuning.

These PDs are connected to two ONET2804TLP four channel limiting TIAs, rated to operate up to 28 Gbps. All 3 dies are wirebonded to an aluminum nitride (AlN) interposer. The PIC is a significantly thicker die than the TIAs. To keep the wirebonds short, the PIC was placed in a cavity in the interposer. The interposer is assembled on a small block of aluminum, which is mounted on a thermoelectric cooler (TEC). While typically TECs are used to stabilize the temperature of a component, in this work we use the TEC to emulate environmental temperature changes to the PIC.

This assembly of PIC, TIA, and interposer is wirebonded to a printed circuit board (PCB), constructed using FR408HR material. The PCB fans out the controlled impedance RF traces to edge-launched SMA connectors. The PCB also provides

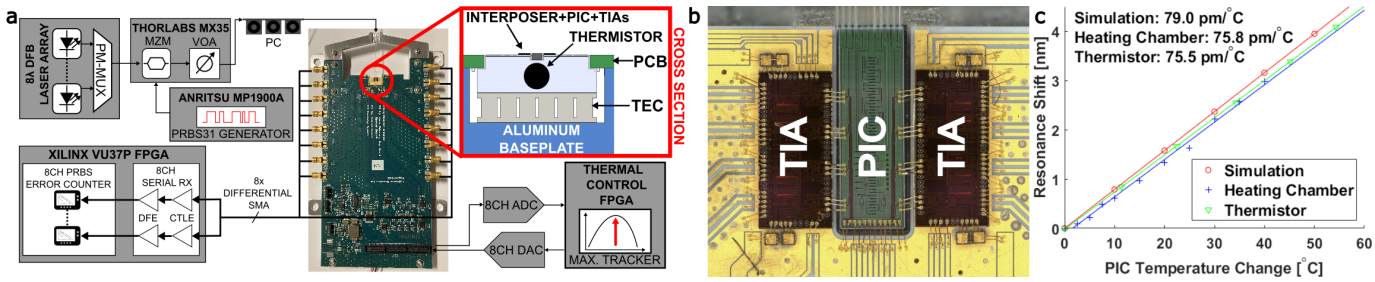

Fig. 1. **a)** System diagram of the experiment, showing a cross section of the PIC and TIAs on an interposer with the TEC and thermistor and the other main components and connections of the system. **b)** Micrograph of the PIC and TIAs wirebonded to the AlN interposer. **c)** Simulated and measured resonance shift as a function of temperature change show strong correlation.

access to the TIAs management interface and the control signals to the PIC.

To thermally stabilize the MRRs, an FPGA reads the average power from the TIAs' received signal strength indicator (RSSI) signals through an eight channel analog-to-digital converter (ADC), and sets a control voltage on the MRRs' integrated heaters through eight digital-to-analog converters (DACs).

When the receiver module is initialized, each filter-channel must first be assigned to its unique wavelength. The integrated thermal tuner offers a tuning range of at least one full FSR ($\sim$26 nm), covering several operational wavelengths. This offers reprogrammability and flexibility, but demands a non-trivial wavelength assignment algorithm. As a reference, the received power on each PD is measured while the MRRs are not locked to any wavelength. When an MRR is moved onto a wavelength, the subsequent MRRs on the optical bus will only see a significantly attenuated remainder of that wavelength. If an MRR is placed on an already occupied wavelength, its RSSI will increase much less than if it was an available wavelength. Thus, by enforcing a minimum increase of the RSSI, we can ensure each MRR is set to a unique wavelength. In this system's case, by automatically assigning each MRR sequentially to its designated location, we were able to reliably initialize the PIC. After initialization is done, the stabilization loop is enabled.

To keep each MRR locked to its assigned wavelength, the FPGA implements a control loop that continuously maximizes the RSSI signals. This is schematized in Fig. 1a. To track the maximum optical power, the control FPGA measures the RSSI at its current heater voltage. It then makes a small step up and down on the heater voltage, measuring the RSSI each time. By repeating this process and selecting the voltage at which RSSI was highest each time, it can track ambient temperature changes. This process is executed for each MRR. The choice for the size of these voltage steps is important. Too large of a step will disrupt the optical signal, and too small means the measured signal will be smaller relative to the noise and limit how fast the system can track changes. To avoid noise spikes, several samples are taken and averaged during each step. In our system an empirically determined value of 336 μV proved sufficient to create a system capable of tracking ambient changes and maintaining lock on all rings. In more sensitive systems, designers could consider making the voltage step linear with the dissipated power, which optimizes this trade off for a wider range of heater voltages. Alternatively, a version of a lock-in amplifier can be constructed by dithering the heater signal. This then allows for the implementation of a standard PID controller to maintain the maximum RSSI signal.

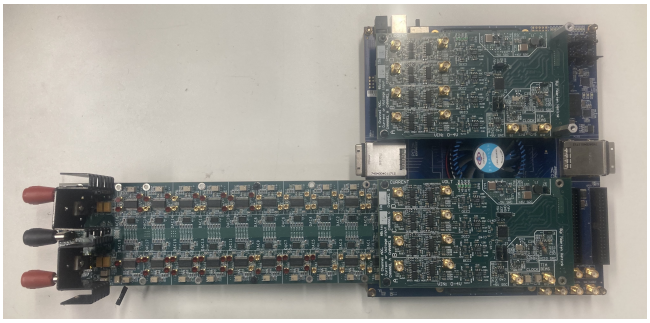

Fig. 2. Pictured are the DAC, ADC, and control algorithm execution boards. The blue PCB, underneath the green PCBs, is an FPGA board used for running the thermal control algorithm. The two short, green PCBs directly above the FPGA board are custom ADC boards, which convert the TIAs' buffered output analog RSSI signal. The longer green PCB extending to the left of the FPGA board is the custom DAC board, which generates the analog control voltages applied to the integrated heaters.

The system's performance was measured using an eight-wavelength Distributed Feedback (DFB) laser array with a nominal wavelength spacing of 150 GHz centered around 1550 nm. The laser lines are combined onto a single fiber using a polarization maintaining multiplexer. Then, all eight wavelengths are modulated with the same pseudorandom binary sequence of length $2^{31}-1$ (PRBS31) from a pattern generator using a broadband Mach-Zehnder Modulator (MZM). The MRRs in the PIC demultiplex all wavelengths, which are then captured by the PDs and TIAs. The output of the TIA is a differential 100 Ω interface, suitable to connect to the high speed serial interfaces of a Xilinx Ultrascale+ FPGA. This second FPGA implements standard signal equalization and an eight channel, parallel pattern checker. The pattern checker can recognize the standard PRBS31 signal pattern and count how many bits are received and how many errors occurred,

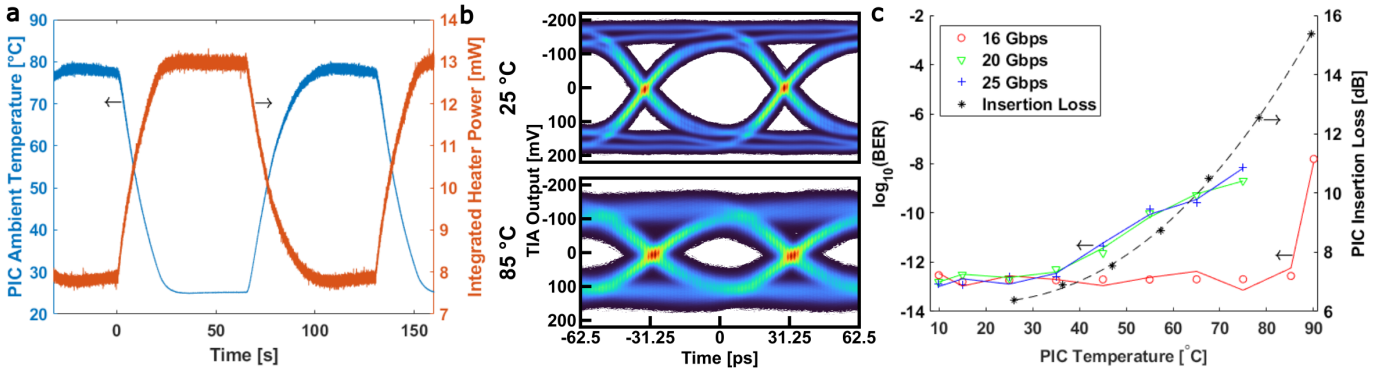

Fig. 3. **a)** Shows the measured PIC temperature and the power dissipated in one of the MRRs during thermal cycling, with a maximum of rate of 3.1 °C/s. Data is transmitted at 16 Gbps and no errors were detected during the entire cycle. **b)** Measured eye diagram of a 16 Gbps PRBS31 signal at 25 °C (top) and 85 °C (bottom). **c)** BER at different data rates measured over wide range of temperatures, set using the TEC. The dashed line shows the PIC's insertion loss, measured outside the MRRs' resonance, increasing at high temperatures, likely due to thermal expansion in the fiber-attach.

thus enabling us to measure the BER of each channel. We can also connect other test equipment to the TIAs' data outputs. For example, we use a real-time oscilloscope to measure an electrical eye diagram.

III. Temperature Calibration

To ensure the thermistor accurately reflects the temperature of the MRRs we calibrated the resonance shift as a function of the thermistor's reading with a simulation in Lumerical's Finite-Difference Time-Domain (FDTD) simulator, and by measuring the resonance shift as a function of temperature in a controlled heating chamber, with results shown in Fig. 1c. Both the simulation and heating chamber results track the thermistor's reading closely. Using the thermistor we measure that the resonance shifts 75.5 pm/°C, compared to the simulation's 79 pm/°C, and the heating chamber measurement's 75.8 pm/°C. This shows that the thermistor accurately reflects the actual temperature of the integrated components on the PIC, with an error <0.4 °C when tuning the MRRs over 80 °C.

IV. System Performance

Using a TED200C TEC controller, we cycle the PIC temperature between 25 and 80 °C. Fig. 3a shows the temperature of the PIC measured by the thermistor and power dissipated in the heater of an MRR. When the PIC temperature is high, the heater power is low. When the PIC temperature decreases, the control system increases the heater power to compensate and maintain a fixed temperature of the MRR. While cycling the temperature, we also transmitted a 16 Gbps signal to the receiver and received no errors inside the 25-80 °C range, thus confirming the thermal control was able to track the change in the PIC's temperature, with a maximum achieved rate of 3.1 °C/s. The limit for the rate of change was the heat transfer capacity of the used TEC.

Fig. 3b shows the measured eye diagrams of a received 16 Gbps PRBS31 at 25 °C and 85 °C, both with open eyes. The eye captured at 85 °C, however, is clearly degraded. In large part, this is because the insertion loss (IL) through the fiber coupler to the PIC increases for temperatures above room temperature, which is shown in Fig. 3c, most likely due to mismatched thermal expansion of the PIC and fiber array. To verify this, we measure the BER of a 28 Gbps signal as a function of received optical power by using a variable optical attenuator (VOA) as a reference. In this measurement the temperature of the system is held a constant 25 °C. Then we measure the BER and received optical power at various temperatures of the PIC. Fig. 4a shows the results of both measurements. There is a strong correlation between both datasets, indicating that the increased insertion loss at is indeed the main cause of the reduction in BER at higher temperatures.

The critical need for evaluation of the thermal design and structures of a photonic-driven transceiver becomes clear due to this result. There is a clear distinction between the thermal robustness of the fiber array (and overall module) and the controlled PIC itself, with the latter being the focus of this work. When the environmental temperature shift is applied directly to the PIC, as in our measurements, the thermal controls are capable enough that the thermal range is limited only by the requirements of other, non-photonic components. However, when tested in a thermal chamber, insertion loss reached untenable levels at only 55 °C, far below our PIC's inherent limit. This is because, in this case, all elements of the module are heated uniformly and slowly, including the epoxy and fiber array, which for this module were not selected to maximize thermal range. A module intended to maximize thermal range should employ other, broader thermal range fibers and epoxies available off the shelf. These components were not selected for this module due to their increased difficulty of assembly.

Fig. 3c shows that at 16 Gbps the receiver is able to maintain error-free operation over a range of 75 °C, to the author's best knowledge the widest reported operating range for a DWDM link based on MRRs. Error-free operation at 16 Gbps here was evaluated to be a BER $< 10^{-12}$ at a con-

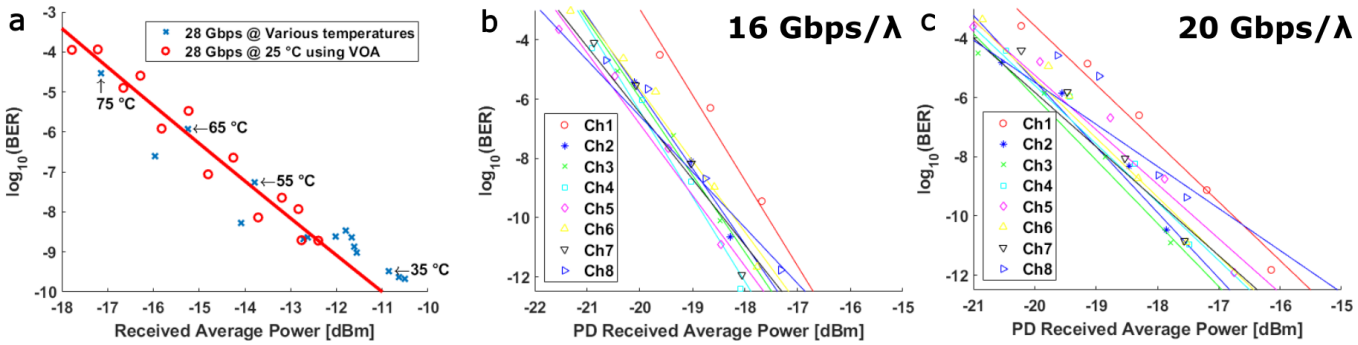

Fig. 4. Measured BER using a PRBS31 signal, with at least 5×10^{12} transmitted bits per data point, shown vs. the optical power received by each photodiode. **a)** Measured BER for a 28 Gbps signal. One set of data points (blue) was captured by only changing the PIC's temperature, i.e. with the VOA disabled. The other set (red) was captured at a fixed 25 °C, but by changing the received power using the VOA. **b)** BER for each channel at 16 Gbps. **c)** BER for each channel at 20 Gbps.

fidence interval of greater than 99 percent. Only above 85 °C does the excess IL from the fiber coupling reduce the link's performance below error-free operation, when heat is applied via the TEC directly to the interposer. At 20 Gbps and 25 Gbps the increased IL reduces the performance more quickly. Both, however, are still able to maintain good performance over a wide range of temperatures. At 25 Gbps, the link maintained a BER $< 10^{-9}$ over at least 65 °C. Using the VOA we measure the performance of each channel on the receiver at 16 Gbps and 20 Gbps respectively, shown in Fig. 4b-c. The results show that all channels exhibit consistent performance.

V. Conclusion

We demonstrate an eight channel DWDM 2.5D integrated SiPh receiver based on MRRs operating error-free at 16 Gbps, uncooled over a record range of 75 °C. We find that the main cause of signal degradation is increased insertion loss in the fiber to PIC coupling, highlighting the importance of taking the targeted thermal environment into account when designing the fiber coupling interface. This demonstration is an important step towards building practical dense MRR-based co-packaged photonic transceivers for next generation compute ASICs, and towards demonstrating the critical nature of thermal analysis of the design of PIC-driven transceivers in hostile thermal environments.

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