Coherent-Perfect-Absorption-based DPSK Demodulator for Silicon Photonics

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Abstract: We demonstrate a fully integrated 10 Gbps novel Si DPSK demodulator using coherent perfect absorption. Our device incorporates a silicon ring resonator, two bus waveguide inputs, monolithically integrated detectors, and operates passively at telecommunication wavelengths, and fits within a mm-scale footprint.

OCIS codes: (130.3120) Integrated optics devices; (060.5060) Phase modulation; (130.4110) Modulators.

1. Introduction

Differential-phase-shift-keying (DPSK) modulation format has recently become of interest for on-chip optical communication systems. This interest is due to its ~ 3-dB improvement in receiver sensitivity in comparison to an intensity modulated direct detection (IMDD) systems, thus enabling increased system margin and reduced input power to the fiber spans and an increasing length of the fiber link[1]. Because of its low-cost manufacturing, high yields, and seamless integration with electronics, it is possible to use Si photonics for on-chip demodulation of DPSK signals [2]. In this connection, [3], a DPSK demodulation scheme based on a ring resonator has been proposed recently, using a phenomenon known as coherent perfect absorption (CPA). In this approach, manipulation of internal field interference *via* critical coupling of the ring with bus and receiver waveguide will lead to coherent control of absorption in such a system [4-6]. CPA based devices have the advantages of independent switching of adjacent resonances, direct heterodyne detection, and smaller footprints [5]. Here, we demonstrate a fully integrated on-chip DPSK demodulator, which modulates at 10 Gbps. These devices have the potential to have a better optical signal-to-noise ratio than IMDD systems. The fundamental principle behind this photonic circuit can be extended to other formats of integrated demodulators.

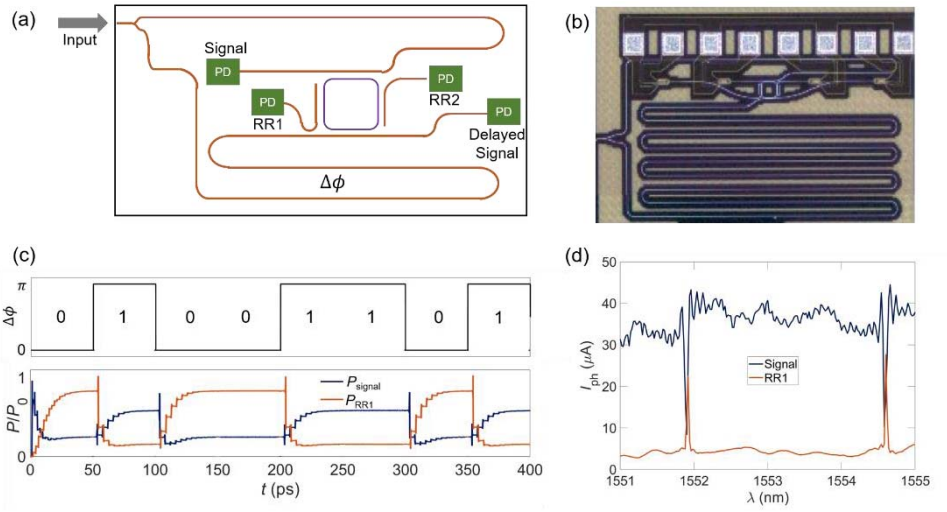

Fig. 1. (a) Schematic diagram of the photonic chip. (b) Optical microscope image of a single 10 Gbps device (c) Simulated DPSK bit sequence and resultant power absorption. (d) Measured photocurrent vs. wavelength for signal and RR1 port for a device with 434 nm bus and ring gap.

2. Device Physics and Characterization

In Fig. 1(a), we show a schematic diagram of the layout of the chip. In addition, Fig. 1(b) shows an optical microscope image of a single device, which has been fabricated by *A*-Star, IME, Singapore. The waveguide and the ring are comprised of oxide-clad Si channel waveguides with cross-sectional dimensions of $500\,\text{nm} \times 220\,\text{nm}$. The input light is evenly split into two signals using a Y- branch and a delay line is used to impart a relative phase delay ($\Delta\phi$) of one bit slot. Thus, the corresponding delay length ($\Delta L = c\Delta T/n_g$) for $1/\Delta T = 10$ Gbps is $\Delta L \approx 7.2$ mm with a waveguide group index $n_g = 4.14$ at $\lambda = 1.55\ \mu$m. The two arms are then recombined in the ring, resulting in detected light in RR1(Ring Resonator 1) if there is no phase shift between bit slots ($\Delta\phi = 0$), or detected light in the photodiodes for signal if a phase shift ($\Delta\phi = \pi$) is present. The ring loss in our CPA scheme is due to coupling loss from the two bus waveguides that connect to RR1 and RR2; the latter replace the absorbing material typically used for CPA [5]. Figure 1(c) shows 2D FDTD simulations of an arbitrary eight bit sequence that was launched into the structure, resulting in the powers as shown for the photodiodes labeled signal and RR1 in Fig. 1(a). For detection of the DPSK signals, four identical Ge *p-i-n* photodiodes (PD) are incorporated onto the chip. Eight Al contacts have been fabricated to measure the electrical photocurrent out of the chip. The transmission spectrum of the ring resonator is shown

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in Fig. 1(d). The free spectral range as measured from the spectrum is 2.68 nm and the Q-factor as measured from the resonant wavelength and linewidth of the transmission dip is 3×10^4.

3. Results and Discussions

In order to evaluate our demodulator circuit, the eye diagrams of the received signal were measured using the experimental setup outlined in Fig. 2(a). In this set up, a pulse pattern generator (PPG) is used to generate a random bit sequence with a bit pattern length of $\mathbf{2^{15} - 1}$ and a peak-to-peak voltage of 0.95 V at a particular clock frequency set by the clock signal generator (CSG). The bit sequence is fed to the phase modulator (PM) through a RF amplifier (RFA). RF amplification is required since the voltage required for the phase modulator for a $\boldsymbol{\pi}$ phase shift exceeds that available from the PPG; i.e., 7 V for the former *vs* 2 V for the latter. The phase modulator modulates the input optical phase based on the bit pattern. The tunable laser source (TLS) is fixed at a resonant wavelength of 1551.88 nm. For a ring of a given radius, the resonant wavelength leads to the best performance for demodulation. The light then passes through the chip so as to demodulate the encoded signal. The photodiodes are reverse biased at 1.34 V through a bias-tee for high speed operation. Also, the laser light is amplified using an Er-doped fiber amplifier (EDFA) and optical grating filter (OGF) before being input to the chip.

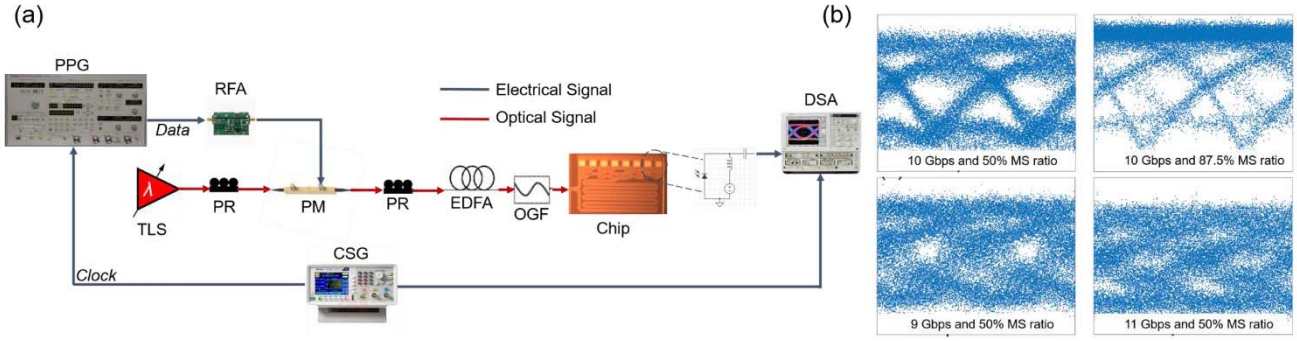

Fig. 2. (a) Experimental setup for eye diagram. (b) Eye diagrams for various data rates and mark/space (MS) ratio. Top left: 10 Gbps data rate and 50% MS ratio. Top right: 10 Gbps data rate and 87.5% MS ratio. Bottom left: 9 Gbps data rate and 50% MS ratio. Bottom right: 11 Gbps data rate and 50% MS ratio.

A typical eye diagram after demodulation is shown in the top left of Fig. 2(b). Open eyes were obtained at a data rate of 10 Gbps and mark/space (MS) ratio of 50%. The eye amplitude is measured to be 12.47 mV. Note the rise and the fall times of this eye are ~0.09 ns. These settings thus limit the device data rate to ~10 Gbps. This speed limitation comes from stabilization time of the ring and the LC or RC constant of the external electrical measurement system. Since DPSK demodulation operates by decoding the message from phase difference of successive bits, it results in a higher number of '1' bits than that of '0' bits as shown in the top right eye diagram of Fig. 2(b) for a MS ratio of 87.5%. Also, as the data rate deviates from the optimal rate, the eyes degrade and appear more closed and distorted as shown in the bottom two figures in Fig. 2(b) for data rates of 9 and 11 Gbps. The minimum BER and maximum extinction ratio occur at the designed data rates, i.e., 10 Gbps, which demonstrates the applicability of our device for high speed data rates. Designs for 20 Gbps designed have been fabricated and await high-speed testing.

4. Conclusion and Future Work

The above results demonstrate the robustness of our DPSK demodulator at different input levels. Note that this characterization of this monolithic integration of the PD with passive a CPA DPSK demodulator is done without the use of post chip electrical amplification and in fact, it is anticipated that the performance of the DPSK device can be further improved with the help of post processing. More generally, our results show clearly that coherent absorption can be used to realize a functional and robust demodulator method for high-speed data transport. Further our results show that this device is readily fabricated in a commercial foundry.

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