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Differential phase-shift-keying demodulation by coherent perfect absorption in silicon photonics

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We demonstrate a novel differential phase-shift-keying (DPSK) demodulator based on coherent perfect absorption (CPA). Our DPSK demodulator chip device, which incorporates a silicon ring resonator, two bus waveguide inputs, and monolithically integrated detectors, operates passively at a bit rate of 10 Gbps at telecommunication wavelengths, and fits within a mm-scale footprint. Critical coupling is used to achieve efficient CPA by tuning the gap between the ring and bus waveguides. The device has a vertical eye opening of 12.47 mV and a quality factor exceeding 3×10^4 . The fundamental principle behind this photonic circuit can be extended to other formats of integrated demodulators. © 2018 Optical Society of America

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Differential phase-shift keying (DPSK) has become a promising modulation format for on-chip optical communications. It offers several key advantages for data communication systems, including improved resistance to nonlinear effects and a ~ 3 dB enhanced sensitivity over that of intensity-modulated direct detection (IMDD) systems [1,2]. It also offers a relatively high extinction ratio and dispersion tolerance. These advantages have led to DPSK-based transceivers being actively considered for short-haul optical communication systems. Many approaches to DPSK demodulation have been implemented, which include controlling the birefringence of a fiber loop mirror filter [3], employing a delayed path-length-based Mach-Zehnder interferometer (MZI) [4], and using a compact preamplified receiver based on Gaussian filtering [5].

These advantages have led to the growing interest in moving toward a fully integrated chip-based system for DPSK (de)modulation. As a materials platform, silicon is particularly attractive due to its great potential for high-quality large-scale systems [6–8]. Silicon-based microring (de)modulators, switches, and filters, fabricated in silicon-on-insulator (SOI) platform, have been demonstrated previously [9–12]. Recently, a Si photonic DPSK demodulation scheme based on ring resonators (RRs) has been proposed. This scheme uses coherent perfect absorption (CPA) [13], where absorption in such a system can be coherently controlled by manipulating internal field interference by tuning the absorption and scattering loss of the ring resonator, which in turn modifies the critical coupling of the ring with bus and receiver waveguides [14,15]. The notion of critical coupling has applications in diverse fields such as light-matter interaction in 2D layered- and plasmonics-based materials [16,17]. Such CPA-based devices have the advantages of independent switching of adjacent resonances and direct heterodyne detection [14] and compared to other demodulation schemes, such as MZIs, require lower driving power, have smaller footprints of the fabricated devices, and are easy to fabricate into arrays, which is essential for wavelength division multiplexed (WDM) systems [11]. Since these devices are compatible with CMOS foundries, they can be a significant component for all-optical circuits, and utilizing carrier injection through applied bias [10], wavelength tunability can be achieved by modifying the critical coupling condition.

Previously, we proposed a CPA-based integrated optical modulator using a ring resonator [14] and experimentally demonstrated a similar racetrack-shaped resonator in SOI platform at telecom wavelengths [15]. Here, we report the fabrication and testing of a *fully* integrated DPSK demodulator optical circuit with *on-chip* Y-splitters, delay line (DL), and photodetectors, which was conceptually proposed in [18]. The chip is

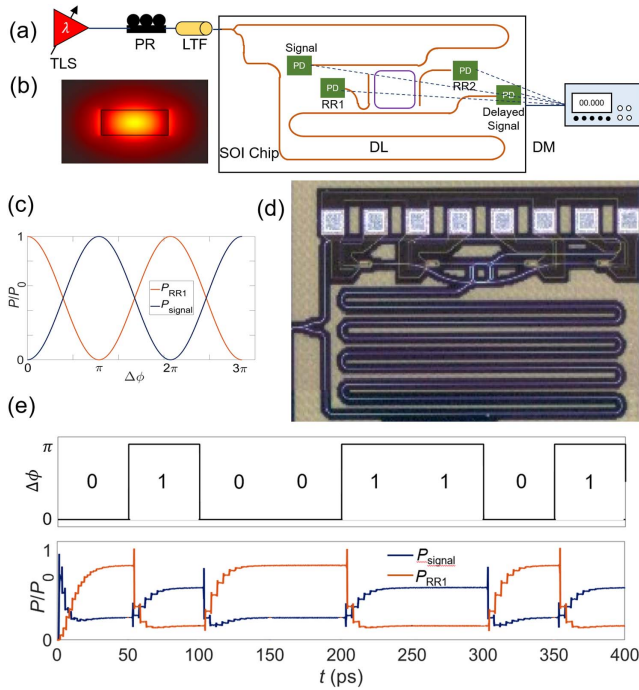


Fig. 1. (a) Schematic of experimental setup. TLS, tunable laser source; LTF, lens-tapered fiber; PR, polarization rotator; DL, delay line; PD, photodiode; DM, digital multimeter. (b) Quasi-TE waveguide mode profile at 1550 nm. (c) Optical microscope image of the device. (d) Calculated power transmission through the signal bus and the ring resonator as a function of relative phase shift ($\Delta\phi$). (e) Theoretical DPSK bit sequence and simulated resultant power absorption. Blue curve: power through signal bus; red curve: power inside ring.

designed for a bit rate of 10 Gbps at C-band communication wavelengths using a 1-bit integrated DL between the two bus waveguide inputs of the ring resonator. We measure this system at 10 Gbps and quantify its performance as a function of bit rate and symbol duty ratio (DR). A schematic layout of the experimental setup is shown in Fig. 1(a). In particular, the input to the ring resonator is evenly split into two signals, with a phase shift ($\Delta\phi$) introduced into one of them by a DL. The two signals are then coupled to the ring through the two bus waveguides. The mode profile in each waveguide is shown in Fig. 1(b). To achieve efficient power transfer between the ring and the waveguide, we must achieve the critical coupling condition [19] that occurs when steady-state power coupling to the resonator from the two bus waveguides ($2\gamma_c$) equals the steady-state power loss rate inside the ring due to material absorption and scattering loss (γ_i). Under this condition, the transmitted signal drops to zero. While in our previous work [15], we achieved this condition by tuning γ_i through Si⁺ implantation inside the resonator itself, in this newly fabricated chip, we achieve it by tuning γ_c through different gap sizes between the bus waveguides and the ring.

From temporal coupled-mode theory [19], the steady state power transmission through any of the signal waveguides is [14]

$$P_{\text{signal}} = \frac{P_0}{2} \left(\frac{\gamma_c^2 + \frac{\gamma_i^2}{4} - \gamma_c \gamma_i \cos(\Delta\phi) + \Delta\omega^2 \pm 2\gamma_c \Delta\omega \sin(\Delta\phi)}{\Delta\omega^2 + \frac{1}{4}\gamma_{\text{tot}}^2} \right), \quad (1)$$

where $\Delta\omega = \omega - \omega_0$, ω is the angular frequency, ω_0 is the resonant angular frequency, and $\gamma_{\text{tot}} = 2\gamma_c + \gamma_i$ is the total loss rate of the cavity. Under critical coupling ($\gamma_i = 2\gamma_c$) and on-resonance ($\Delta\omega = 0$) condition, Eq. (1) simplifies to [13,14,20] $P_{\text{signal}} = (P_0/2) \sin^2(\Delta\phi/2)$, while the power inside the ring varies as $P_{\text{RR1}} = P_{\text{RR2}} = P_0 \cos^2(\Delta\phi/2)$ [Fig. 1(c)]. Therefore, we make use of differential detection by measuring $\Delta\phi$ between successive modulated phases of the received signal. The bit rate ($1/\Delta T$) is related to the phase difference through the length of the DL (ΔL), and thus $\Delta\phi = 2\pi c \Delta T / \lambda n_g$, where c is the speed of light, λ is the resonant wavelength of the ring, and n_g is the waveguide group index. The two signals are then coupled inside the ring resonator such that based on the value of $\Delta\phi$ of two successive bits, the demodulator will have power at either the bus waveguide or the ring itself.

Our device was fabricated at the Singapore Institute of Microelectronics. The structure is based on standard SOI technology consisting of a 220-nm-thick silicon device layer and a 2- μm buried oxide (SiO₂) layer. The entire chip is cladded with SiO₂. Figure 1(d) shows an optical microscope image of a representative example of a 10-Gbps device. RSoft FemSIM yields a loss coefficient $\alpha = 0.049 \text{ cm}^{-1}$ of the fundamental waveguide quasi-transverse electric (TE) mode, which occurs due to material absorption. To first-order approximation, $\gamma_i = 2\pi R \alpha v_g / L_{\text{tot}}$ and $\gamma_c = \sin^2(\kappa L_c) v_g / L_{\text{tot}}$, where R is the radius of the ring, v_g is the group velocity, L_{tot} is the total linear length of the waveguide, L_c is the coupling region length, and κ is the bus-to-resonator coupling coefficient [21]. For a coupling gap of 434 nm, the device is nearly critically coupled with $\gamma_i \approx 2.3\gamma_c$. The calculated delay based on the waveguide geometry and dispersion was ~ 0.1 ns, corresponding to a bit rate of 10 Gbps.

As shown in Fig. 1(a), a Y-branch and DL are used to split the input signal into the two paths having a relative delay of one bit. The waveguide and the ring are comprised of oxide-clad Si channel waveguides with cross-sectional dimensions of 500 nm \times 220 nm. In Fig. 1(b), we plot the mode profile of the fundamental TE mode of the Si waveguide, calculated using RSoft FemSIM, and we use this to compute the waveguide group index ($n_g = 4.14$ at $\lambda = 1.55 \mu\text{m}$). Thus, the corresponding delay length ($\Delta L = c \Delta T / n_g$) for $1/\Delta T = 10$ Gbps is $\Delta L \approx 7.2$ mm. For detection of the DPSK signals, four identical Ge p-i-n photodiodes are incorporated onto the chip because of their high speed, broad detection spectrum, and the compatibility of their processing (primarily thermal management in growth) with Si CMOS technology. The Ge-photodiode length has been reduced to increase the bandwidth of these photodetectors. Eight Al contacts were fabricated to measure the electrical photocurrent out of the chip. There are four 10-Gbps devices with varying gaps from 404 nm to 494 nm between the bus waveguides and the ring. This results into varying coupling coefficient (γ_c) values ranging from 2 cm^{-1} to 6 cm^{-1} .

To investigate *a priori* the DPSK demodulation behavior of our proposed structure, we perform 2D-finite-difference time-domain (FDTD) simulations (RSoft, FullWAVE) using the on-chip dimensions of the ring. We launch two fundamental modes ($\lambda = 1.55 \mu\text{m}$) having a phase difference ($\Delta\phi$) in the two bus waveguides. An arbitrary 8-bit sequence is created by changing $\Delta\phi$ between 0 and π . We use temporal and spatial grids of 0.2 fs and 0.1 μm , respectively. The monitors for collecting the outputs as a function of time are placed on the through and drop ports at a distance of 37.75 μm from the center of the waveguides,

resulting in the powers shown [Fig. 1(e)] for the photodiodes labeled signal and RR1 in Fig. 1(a). For $\Delta\phi = 0$, the two inputs are identical, and the ring is in CPA resonance, resulting in power absorption within the ring and nothing transmitted out of the signal bus. For $\Delta\phi = \pi$, the ring is not in CPA resonance, and thus the power of the ring decreases and the transmitted power in the signal bus increases. Thus, for DPSK signals, where the bit information is stored inside the relative phase of the successive bits, this device can extract the information using the DL and its RR-CPA response. The step response in the power signal corresponds to the stabilization of the round-trip transit time of the electric field inside the ring resonator.

Ideal system-level simulations are then carried out using RSoft OptSim (Fig. 2). We use a T-flip flop (TF) to convert a pseudo-random bit sequence (PRBS) into DPSK-encoded signal. A radio frequency (RF) waveform is used to drive the phase modulator (PM) that encodes the bit pattern into the phase of the continuous-wave (CW) laser light. After passing through a 50:50 Y-splitter (YS) and DL, the two signals are injected to a resonator. The resonator comprises two couplers (C1 and C2), two waveguides (W1 and W2), and an optical attenuator (L). The attenuation coefficients of the couplers and attenuators follow the critical-coupling condition ($\gamma_i = 2\gamma_c$). The combined length of the couplers, waveguide, and attenuator matches the circumference of our resonator, i.e., 214.25 μm . In addition, the waveguides have effective index of 2.43 at a wavelength of 1.55 μm . The output of the resonator is fed into an avalanche photodiode (PD) that converts the output optical signal into electrical signal. After passing through a low-pass filter (LPF), the signal is amplified through a transimpedance amplifier (TIA). The left inset in Fig. 2 shows the input and output bit streams ensuring that the demodulator circuit is correctly decoding the DPSK-encoded signal. The right inset in Fig. 2 shows the resultant eye diagram.

Prior to high-frequency testing of DPSK demodulation, the transmission spectrum of the device was measured using a CW tunable laser source (TLS) (APEX AP3350A). The input light from the TLS was edge coupled onto the chip using lens-tapered fiber (LTF). An inverted taper of 180 nm width was used to couple the light from the fiber to the 500-nm-wide waveguide. The photocurrent was measured using a MATLAB program to control an APEX AP1000-8 Mainframe controller with an Agilent 34410 A multimeter.

The resultant photocurrent transmission spectra are shown in Fig. 3 for the signal and the RR1 ports. With $n_g = 4.14$ and a circumference of 214.25 μm , the free spectral range (FSR) of the ring resonator is 2.7 nm at 1.55 μm . The calculated Q-factor ($= \tau\omega_0/2$) for the resonator is obtained from FDTD

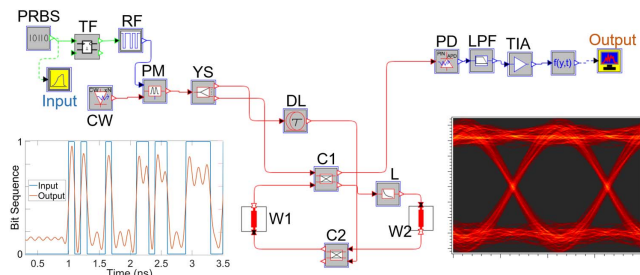


Fig. 2. Schematic of the DPSK demodulation system. Left inset: input bit pattern and the output electrical signal. Right inset: resultant eye diagram. Abbreviations: see text.

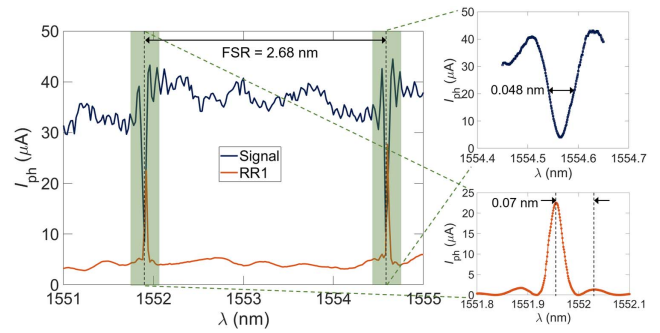


Fig. 3. Measured photocurrent versus wavelength for the signal and the RR1 port for a 10-Gbps device with a 434-nm bus and ring-gap. Top inset: one resonant dip of the delayed signal port, to calculate Q . Bottom inset: photocurrent inside the ring, to calculate the wavelength change for a 2π phase shift.

simulation to be 2.8×10^4 . In Fig. 3, the measured FSR is 2.68 nm for a device with 434 nm gap. The top inset in Fig. 3 shows a dip in the delay signal in the green shaded region of the figure with a 0.001-nm resolution. The measured Q-factor of the ring ($= \lambda_{\text{res}}/\Delta\lambda$) as seen in the upper right inset in Fig. 3 is 3.2×10^4 , in good agreement with the calculated value. The wavelength dependence of the phase difference between two arms is calculated to be -24.6π rad/nm, based upon the usual expression $\frac{\partial}{\partial\lambda}\Delta\phi = -\frac{2\pi\Delta d}{\lambda^2}n_g$. Thus, the phase difference changes by 2π every 0.08 nm of wavelength, in agreement with the measured phase change of 0.07 nm (Fig. 3 bottom inset).

To assess the quality of our demodulator circuit, we measured the eye diagrams of the received signal. The experimental setup for eye extraction is shown in Fig. 4. In this setup, a pulse pattern generator is used to generate a random bit sequence with a bit pattern length of $2^{15} - 1$ and a peak-to-peak voltage of 0.95 V at a clock frequency, as set by the clock signal generator. The bit sequence is fed to the phase modulator through a RF amplifier. The phase modulator modulates the input optical phase based on the bit pattern. The laser light is fixed at a resonant wavelength of 1551.88 nm. The light then passes through the chip so as to demodulate the encoded signal. The photodiodes are reverse biased at 1.34 V through a bias-tee for high-speed operation. Also, the laser light is amplified by ~ 4 dB using an Er-doped fiber amplifier (EDFA) and optical grating filter prior to input to the chip.

In Fig. 5(a), we plot the eye-opening amplitudes for data rates of 9–11 Gbps. Because of the structure of the CPA-based DPSK demodulator, the output signal can be seen as a combination of the band-passed duobinary signal at drop port and the alternate mark inversion signal at the through port.

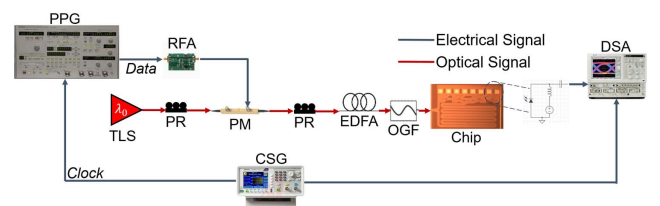


Fig. 4. Eye-diagram measurement. PPG, pulse pattern generator; RFA, RF amplifier; TLS, tunable laser source; PR, polarization rotator; PM, phase modulator; EDFA, Er-doped fiber amplifier; OGF, optical grating filter; CSG, clock signal generator; DSA, digital serial analyzer.

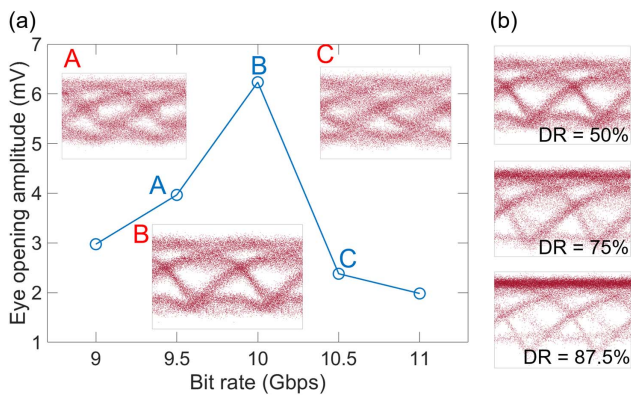


Fig. 5. (a) Tolerance of DPSK demodulator circuit to varied signal bit rate. (b) Eye diagram with different duty ratios of 50%, 75%, and 87.5%. The minimum BER and maximum extinction ratios occur at the designed symbol rate of 10 Gbps.

Three typical eye diagrams after demodulation are shown in the insets in Fig. 4(a). As mentioned previously, the device was designed for 10 Gbps. As the data rate deviates from this optimal rate, the eyes degrade and appear more closed and distorted. Thus, the demodulation scheme exhibits better tolerance to lowered bit rates compared to higher bit rates, as was also demonstrated in [11]. The rise and the fall times of the eye for optimum rate (10 Gbps) are ~ 0.09 ns. These settings thus limit the device data rate to ~ 10 Gbps due to the stabilization time of the ring and the time constants of the external electrical measurement system. The minimum noise and maximum extinction ratio occur at the designed data rate, i.e., 10 Gbps, which demonstrates the applicability of our device for high-speed data rates.

In addition to the frequency response of the eye diagrams, we also investigated their response to the relative abundance of the symbols in order to ensure that our device is demodulating differentially encoded signals rather than basic phase-shift encoded signal. The top eye diagram in Fig. 5(b) is obtained with a DR, i.e., ratio of “1” bit to “0” bit in the randomly generated bit pattern of 50%. Operation under different DRs was then examined, namely, 75% and 87.5% by increasing the number of “1” bits in the input bit stream. Since DPSK demodulation operates by decoding the message from phase difference of successive bits, it results in a higher number of “1” bits than that of “0” bits, as shown in the bottom two eye diagrams in Fig. 5 for DRs of 75% and 87.5%, respectively. The resulting dependence of measured extinction ratio on the occupation ratio of bit 1, as shown in Fig. 5, is weak. Finally, we attribute the rippled top (bit 1) and bottom (bit 0) of the eye diagrams to the electrical stabilization time of the ring (see also Ref. [22]). This effect can be stabilized with an electrical filter. Our results demonstrate the robustness of our DPSK demodulator at different input levels. Note that this characterization of this monolithic integration of the PD with a passive CPA DPSK demodulator is done without the use of post-chip electrical amplification. In addition, it is anticipated that the performance of the DPSK device can be further improved with the help of post processing. More generally, our results show clearly that CPA can be used to realize a functional and robust demodulator for high-speed data transport.

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