Energy Efficiency Analysis of Comb Source Carrier-injection Ring-based Silicon Photonic Link

Yanir London*, Thomas Van Vaerenbergh, Anthony J. Rizzo, Peng Sun, Jared Hulme, Geza Kurczveil, Ashkan Seyedi, Binhao Wang, Xiaoge Zeng, Zhihong Huang, Jinsoo Rhim, Marco Fiorentino, and Keren Bergman

***Abstract*—Current electronic interconnections in high performance computing (HPC) systems are reaching their limit in supporting high data traffic demands. Dense wavelength-division multiplexed (DWDM) links have gained interest as they can potentially alleviate these interconnect bandwidth demands while also lowering the cost and energy consumption compared to traditional electronic links. In this paper we present an analysis of a ring-based DWDM silicon photonic (SiP) link architecture with a comb laser source and p-i-n photodetectors. Specifically, we consider microring resonators (MRRs) with narrow bus waveguides and carrier-injection ring modulators. We propose a new method to select the optimal comb source setting to minimize the laser power consumption at a particular data rate. Additionally, we leverage power penalty models supported by measurements to estimate the effective received optical power at the receiver input of each of the DWDM channels which yields a bit error rate (BER) of 10^{-12} or lower. We show that the analyzed comb source has the lowest power consumption per channel for 24 consecutive lines. For these comb settings, the maximum channel data rate of non-return to zero on-off keying (NRZ-OOK) signals is 22 Gbps, and the minimum energy consumption is 3.28 $\frac{\text{pJ}}{\text{bit}}$.**

I. INTRODUCTION

THE continuous rise of data-intensive applications is pushing the data traffic demands of interconnects in high performance computing (HPC) systems to new limits [1]. To support the bandwidth requirements of next generation HPC systems, electronic interconnections are expected to be replaced by dense wavelength-division multiplexed (DWDM) links. DWDM optical links enable significantly higher bandwidth transmission with lower cost, latency, and loss compared to electronic interconnections. A promising technology for DWDM links in next generation HPC systems is the emerging silicon photonics (SiP) platform. SiP provides a high-bandwidth, energy-efficient, and CMOS integration compatible technology [2]. To minimize the package size and the power consumption it is necessary to consider different light sources for a holistic link analysis. In typical commercially available wavelength-division multiplexed (WDM) systems, the wavelengths are produced by an array of single-wavelength continuous wave (CW) lasers. However, this poses a challenge to meet the packaging size and power consumption requirements. On the other hand, comb lasers are considered to be a promising candidate to replace CW laser arrays as they can produce numerous evenly-spaced tones from a single source. The numerous available comb lines form a cost-effective DWDM source for SiP links in HPC systems. A commonly used method for generating frequency combs is through mode-locking pulsed lasers, where the tones correspond to cavity modes and thus have precise, intrinsic spacing between adjacent supported modes which relaxes the tuning requirements compared to CW arrays. Specifically, mode-locked quantum dot comb lasers are well-suited as SiP link sources due to their relative maturity, small footprint, cost-effectiveness, and chip-level integration [3], [4]. On-chip microresonator-based Kerr combs are also gaining traction as SiP link sources due to their low power consumption and chip-level integration. Integrated microresonator-based Kerr combs in the anomalous dispersion regime are widely investigated, but the reported results have incompatible performance for non-amplified SiP links due to their low conversion efficiency and insufficient comb line power for overcoming the link power penalties [5], [6], [7]. On the other hand, recent studies of microresonator-based Kerr combs in the normal dispersion regime show better conversion efficiency and optical power per comb line that can be suitable for SiP links [8], [9], [10]. However, current demonstrations are done only with an external CW pump source that emits light with power on the order of hundreds of milliwatts. A fully integrated comb solution has not yet been demonstrated. In this work, we used off-the-shelf comb sources to find the maximum aggregated data rate supported by currently available technology. The comb lines can be either modulated by broadband modulators, e.g., electro-absorption modulators (EAMs) and Mach-Zehnder modulators (MZMs) or wavelength selective microresonator modulators, e.g., microring/microdisk modulators and photonic crystal cavity modulators [11]. Broadband modulators in the SiP platform have been widely studied, and PAM4 transmission up to 128 Gb/s with MZMs has been demonstrated [12]. However, in the context of DWDM transmission, the scalability of these modulators is limited by their large footprint and lack of wavelength selectivity. Due to their broadband nature, this class of modulators requires the DWDM comb lines to be demuxed and routed to individual modulators before being recombined for transmission. This architecture has substantially increased complexity and footprint compared to designs based on cascaded microresonators, which leverage wavelength selectivity to remove the need for a demux stage before modulation while boasting a significantly smaller footprint. MRR and microdisk modulators are preferred to

*Corresponding author, email address: yl3931@columbia.edu.

Y. London, A. J. Rizzo and K. Bergman are with the Department of Electrical Engineering, Columbia University, New York, NY 10027, USA.

T. Van Vaerenbergh, P. Sun, J. Hulme, G. Kurczveil, A. Seyedi, B. Wang, X. Zeng, Z. Huang, J. Rhim and M. Fiorentino are with Hewlett Packard Labs, Palo Alto, CA 94304, USA.

photonic crystal cavity modulators for wavelength-selective modulation due to their design maturity and lower sensitivity to fabrication variations. In particular, we are interested in MRRs with a narrow bus width, which are potentially less sensitive to fabrication variations [13], and carrier-injection ring-based modulators due to their high modulation efficiency. On-off keying (OOK) has gained popularity as a modulation format for HPC DWDM interconnects due to its relatively low-complexity hardware requirements to achieve error-free performance and its capability to scale up the aggregated data rate by adding another (wavelength) channel without increasing the driver design complexity, and consequently maintaining the same $\text{pJ} \cdot \text{bit}^{-1}$ level. Higher-order pulse amplitude modulation (PAM) using ring-based modulators has also been demonstrated for high-speed SiP links [14], [15], [16]. However, it requires additional hardware, such as linear drivers, digital processing and forward error correction (FEC), that increase the overall complexity of the DWDM transceiver while the eye opening is lower compared to OOK [17]. Additionally, as the number of channels increases, the hardware complexity grows dramatically, decreasing its appeal for near-term error-free low-energy HPC links. In the design of a comb source-driven ring-based SiP link, it is crucial to consider the interaction between the photonic components to maximize the power budget of the link. We used power penalty models supported by data from our device measurements to estimate the maximum aggregated data rate of the link, and the minimum energy consumption at this aggregated data rate. We found that the analyzed link can support a maximum aggregated data rate of non-return to zero on-off keying (NRZ-OOK) DWDM signals of 528 Gbps with an energy consumption of 3.28 $\frac{\text{pJ}}{\text{bit}}$.

II. Link Budget: Models and Analysis

In this work, we focus our analysis on a cascaded ring-based SiP DWDM link architecture with a comb laser source. A block diagram of the link architecture is shown in Fig. 1. The link consists of photonic components and electronic devices. The photonic components include the comb laser source, grating couplers, cascaded-ring modulators, cascaded-ring filters and photodetectors (PDs), while the electronic devices include the drivers and trans-impedance amplifiers (TIAs). At the transmitter-side, the MRRs are thermally tuned to match consecutive wavelength tones of the comb source. To modulate the data over each of the comb lines, the carrier density inside the ring waveguide is manipulated by the driver, changing the effective index and thus shifting the resonance. The light can be modulated by using either carrier-injection or carrier-depletion in the ring waveguide to change the effective index [18]. A reverse-bias applied on the p-n junction of a carrier-depletion ring results in a wider depletion region which decreases the carrier concentration in the waveguide core, resulting in an increase in the effective index and thus red-shifts the resonance. Conversely, a forward-bias applied on the p-i-n diode of a carrier-injection ring results in injection of electrons and holes into the intrinsic region. This leads to an increase of the carrier concentration within the waveguide core, which decreases the effective index of the silicon waveguide and thus blue-shifts the resonance. As a result of the different physics, carrier-depletion modulator rings have an intrinsically faster response time compared to carrier-injection rings, which results in simpler driver designs at high data rates. However, carrier-injection rings have higher modulation efficiency such that the required driving voltage is significantly lower compared to carrier-depletion rings. At the receiver-side, each of the DWDM channels is filtered by a tuned MRR and detected by a PD followed by a TIA. The objective of this work is to find the link configuration that supports the highest aggregated data rate, and the lowest energy consumption at this aggregated data rate. This requires two different analyses performed sequentially: (i) link budget, and (ii) energy efficiency. The link budget analysis includes the supplied optical power of DWDM lines of the comb laser and the link losses and power penalties (PPs) resulting from the photonic components. The equivalent received optical power (EROP) of NRZ-OOK signal to achieve a bit error rate (BER) of 10^{-12} is then calculated for each of the DWDM channels and compared to the receiver sensitivity. The link is consider to be valid if the worst EROP is above the sensitivity level. The key features of the analyzed link in this work are: (i) a quantum dot-based comb laser, (ii) carrier-injection ring-modulators, (iii) MRRs with non-identical bus-ring waveguide widths, and (iv) p-i-n PDs. We develop a new method to select the optimal comb source settings and by leveraging known power penalty models supported by comb laser and MRR measurements, we estimate the EROP of NRZ-OOK signals at the receiver input of each of the DWDM channels. The models of the photonic components that we have used for our link budget analysis are described below. We suggest a methodology to obtain the photonic component parameters that maximize the aggregated data rate, while the losses and power penalties are minimized.

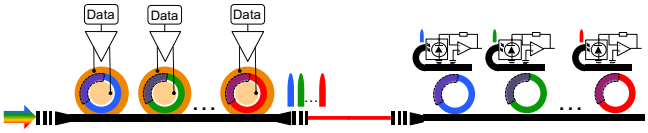

Figure 1. A block diagram of unidirectional SiP DWDM interconnect.

A. Frequency comb source

The formulation of compact models for comb lasers is particularly difficult due to the rich nonlinear dynamics and fabrication deviations that determine the final output spectrum. Without compact models for the source, it is prohibitively inefficient to scan the joint design space of the comb and the link. In lieu of an analytic compact model, we opt to create a database of comb spectra for various parameters, e.g. temperature, supplied current, and saturable absorber bias, which can be characterized and accessed during the link optimization process. For each database entry, the output spectrum from an optical spectrum analyzer (OSA) is searched using a peak finding algorithm to identify the optical power and center wavelength for each comb line. The regions around

each line are then separated and the center wavelength and optical power from peak finding are used as initial guesses to fit each comb line to the spectral line shape with the smallest fitting error (approximated as Lorentzian). The regions are then recombined to recreate the full fitted spectrum, entirely characterizing the comb laser output by a set of Lorentzians for each setting.

The link design space is highly dependent on the capability of the source. Two key considerations are: (i) how many channels the source can provide that overcome the power penalty of the link and (ii) the line spacing provided by the source. The line spacing of a particular comb laser is fixed since the lines correspond to modes of the laser cavity, which poses a restriction on the channel spacing of the link and can introduce added crosstalk for particular architectures. For a given channel count and data rate per channel, the energy consumption per bit for the laser can be calculated by scanning the database to find all possible configurations that satisfy the channel count, i.e., lines above the power penalty of link, and then analyzing the corresponding IV curves to calculate the total power consumption for the given configuration. From this set of satisfying configurations, the one with the lowest power consumption yields the optimal energy per bit for the entire link. However, the power consumption of the laser contributes disproportionately to the total power consumption of the link [19], so choosing a particular link configuration and then searching for the most energy efficient source does not guarantee that the energy consumption per bit is a global minimum. Rather than beginning with the link configuration and searching for a satisfying source, it is useful to first define a metric that captures the optimal energy efficiency of a particular comb configuration. The effective wall plug efficiency (EWPE) is then defined as

$$\text{EWPE} = \frac{\sum_{\text{lines}} P_{\text{optical}}}{P_{\text{electrical}}} < \text{WPE} \tag{1}$$

where WPE is the wall plug efficiency, $P_{\text{electrical}}$ is the total electrical power consumption of the laser and thermoelectric cooler (TEC) and $\sum_{\text{lines}} P_{\text{optical}}$ is the sum of the optical powers over all comb lines above the given power budget, $\mathcal{P}_b$. In our modeling framework, the optical power of the individual comb lines can be quickly obtained by integrating the Lorentzian fits over each region. In the design space of a low-power consumption photonic link with a comb source, the EWPE provides an advantage over the WPE since the electrical to optical conversion for comb lines below the link power budget yields unusable carriers and therefore the conversion efficiency is only of interest for lines above the budget. The EWPE acts as a proxy for the total possible energy per bit of the source (for a given modulation rate) if all potential carriers are used. In [20], regions of operation were identified based on the dependence of consecutive comb lines above a specified link power budget with respect to current and temperature. For stable regions of operation, the power consumption was analyzed for various channel counts to find the configuration that yields the lowest energy per bit. We used an Innolume comb laser with dimensions of $1 \times 0.5 \times 0.2$ mm^3. Figure 2 shows the total power consumption of a particular Innolume comb laser per channel (each of which is above $\mathcal{P}_b = 0$ dBm) for various channel counts when scanning the source over supply current. The circled points indicate the highest effective wall-plug efficiency (EWPE) for a specific channel count, which yields the lowest total electrical power per channel, confirming our figure of merit. Therefore, in the design of an energy efficient link with a specific channel count the comb laser configuration can be selected independently from the other photonic components by taking the supply current setting with the highest EWPE.

The main contributor to the crosstalk penalties at the modulator- and demodulator-side is the nearest "aggressor" channel [19], [21]. In our study, the comb laser has a fixed channel spacing of 0.28 nm such that the difference in power budget performance as a function of the number of available lines is expected to be negligible. Therefore, to maximize the aggregated data rate, we set the supply current to 261 mA, which results in 24 consecutive lines in the range of 1283.38-1289.82 nm, and a total electrical power consumption of 0.476 W. With these settings, the electrical laser power per channel has the lowest value compared to other channel counts.

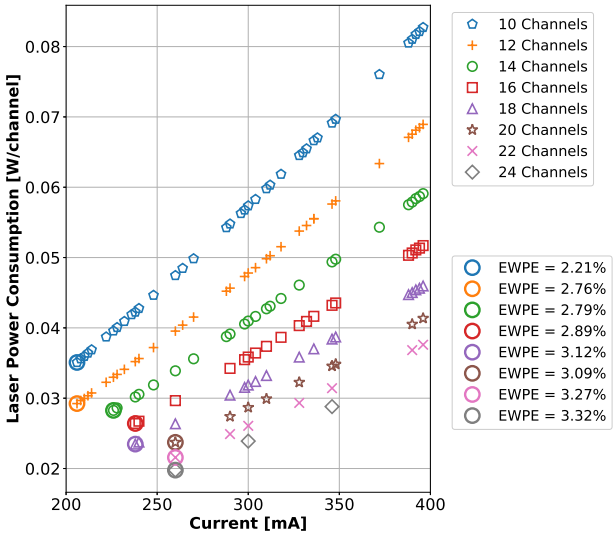

Figure 2. Dependence of Innolume comb laser total electrical power per channel on current for various channel counts with a fixed channel spacing and a $\mathcal{P}_b = 0$ dBm. Circled points indicate optimal energy efficiency for each channel count with respective EWPE values.

B. *Grating coupler*

The SiP link consists of three building blocks: the comb source, cascaded ring modulators, and cascaded ring demodulators. Optical couplers are placed along the link to transfer the light between the different platforms. The positions of the optical couplers in the link are shown in Fig. 1. In this work, the photonic components are designed for wafer-level measurements with grating couplers (GCs), which have reduced mode mismatch compared to edge couplers. Recent progress in design techniques and optical proximity correction

(OPC) enable a reduction of the accessible critical dimensions by using 193 nm deep ultraviolet (DUV) lithography, resulting in improvements of the GC efficiency. In Ref. [22], it is reported that the peak loss of commercially available GCs, which were taped out using a low cost 300 mm SOI substrate and were optimized for 1310 nm, are dependent on the chip location due to etch depth variation across the wafer. The minimum measured GC peak loss is 2.6 dB. On the other hand, [23] recently demonstrated the development of a new design for a single-polarization GC. The transmission spectra of a collection of single-polarization GCs, which were taped out using a 300 mm wafer platform and were optimized for 1310 nm, were measured. It was shown that the new GC design has a median value of the minimum insertion loss of -1.35 dB, and a -1 dB bandwidth of 21 nm. We expect that process improvements will achieve similar light coupling performance in our future photonic device tape-outs. Therefore, in our analysis we assumed a GC with light coupling performance as in [23], where its central wavelength λ_p with the minimum insertion loss (IL) $IL_{\min}$ is located at the center of the DWDM band. The estimated GC insertion loss trend follows a second order polynomial:

$$L_{GC}[dB] = -\frac{IL_{-1\text{ dB}} - IL_{\min}}{(\frac{1}{2}B_{GC})^2}(\lambda - \lambda_p)^2 - IL_{\min}, \quad (2)$$

where λ is the wavelength, B_{GC} is the -1 dB bandwidth with $IL_{-1\text{ dB}}$.

C. Ring-based modulators and demodulators

The high wavelength selectivity and the small footprint of MRRs is desirable for integrated DWDM links. A typical ring-based DWDM link consists of cascaded active- and passive-rings along a bus waveguide at the transmitter- and receiver-side, respectively. Each of the active-rings at the transmitter-side modulates the data over each of the available comb lines, and each of the passive-rings at the receiver-side filters one of the DWDM channels before being detected by the PD. The area of ring-based transmitter (or receiver) chip is determined mainly by the rings size, pads size and spacing, and to a lesser degree, by the fiber mode-field diameter. To minimize the RF mismatch loss, flip-chip assembly is considered. In that case, the RF pad dimensions and spacing depend on the driver bump pad size and bump pad pitch. In the current driver design, the pad length, width and pitch are 40 μm (more details on the driver design are given in Section III-B). Recent works reported on smaller bump pad pitch of sub-10 μm [24], [25]. The mode-field diameter of a single mode fiber is 9.2 μm at 1310 nm[1]. Multiple ring-based transmitters (or receivers) can be fabricated on a single SiP chip. In that case, fiber arrays are required at the optical I/Os. The core pitch spacing between adjacent fibers is limited by the fiber diameter. Therefore, the core pitch spacing of SMF is typically in the range of 127-250 μm.

In the case of ring-based SiP links with p-i-n PDs, the main power penalty contributors are the signal-independent noise (SIN) and the crosstalk impairment [19]. To estimate the eye closure and the received optical power at the PD input, we used the SIN and crosstalk power penalties at the transmitter-side terms given in Ref. [19], and the SIN and crosstalk power penalties at the receiver-side terms given in Refs. [19], [21], respectively. Additionally, we assumed the propagation losses of the light along the bus waveguide are negligible. In our analysis, we considered an add-drop MRR with non-identical bus-ring ridge waveguide widths. At the transmitter-side, the drop port is used for integrated power monitoring and resonance tuning [26]. In addition, in Ref. [13] it is shown that MRRs with a narrower bus waveguide width compared to the ring waveguide width have better phase matching. This results in weaker excitation of high-order modes and better coupling performance that enables larger bus-ring gaps that are less sensitive to fabrication variations.

In the calculation of the power penalties, the channel spacing (0.28 nm) is determined from the comb laser cavity length. In addition, we assumed that at the '0' symbol each of the ring-based modulators is tuned to one of the available comb lines in descending order, and each of the ring-based filters is tuned to the desired DWDM channel. The MRR performance properties of the ring-based modulator at the '0' symbol and the ring-based filter, which are required for the power penalty terms, can be calculated using the terms in Ref. [27] from the round-trip power loss a and the self-coupling coefficients of the input-ring waveguides and ring-drop waveguides, which are denoted by r_1 and r_2, respectively. In Ref. [28], a new behavioral model of SiP MRRs with unequal bus-ring widths was developed. It is shown that the proposed model describes accurately the coupling transfer function matrix of bus-ring directional couplers with non-identical widths. We used this model to extract r_1 and r_2. In Ref. [22], a first order approximation of the MRR round-trip power loss is given by:

$$a^2 = \exp\left(-\alpha L - l_{thru} - l_{drop}\right), \quad (3)$$

where α is power attenuation coefficient of a waveguide, $L = 2\pi R$ is ring round trip length, R is the ring radius, $l_{thru} = A\exp(-b_0 \cdot g_1)$, $l_{drop} = A\exp(-b_0 \cdot g_2)$, g_1 and g_2 are the through and drop gaps, respectively, and A and b_0 are the coupling loss fitting parameters. In [22], it is reported that the fitted waveguide loss is 11.6 dB·cm^{-1} ($\alpha = 2.66$ cm^{-1}), which is higher than the expected losses. The high loss value can be explained by the sidewall roughness. However, the sidewall roughness and as a result the waveguide loss are expected to be improved in future tape outs. We estimated the propagation loss of a straight waveguide at 2 dB·cm^{-1} ($\alpha = 0.4605$ cm^{-1}), and we used Lumerical MODE to calculate the loss of a bent waveguide. The power attenuation coefficient of a silicon (Si, $n_1 = 3.507$) core bent ridge waveguide versus the waveguide radius is shown in Fig. 3(a), where the cladding is silicon dioxide (SiO2, $n_2 = 1.447$), and the ridge waveguide width, waveguide height and slab thickness are $w_{wg} = 450$ nm, $h_{wg} = 300$ nm, and $h_{slab} = 50$ nm, respectively. In Fig. 3(b), the MRR round-trip power loss versus ring radius is shown, where the bent waveguide loss in

[1]Based on Corning SMF-28 Ultra Optical Fiber data sheet, https://www.corning.com/media/worldwide/coc/documents/Fiber/SMF-28%20Ultra.pdf

Fig. 3(a) and the reported coupling losses l_{thru} and l_{drop} in Ref. [22] ($A = 0.0059$ and $b_0 = 4.67$) are considered.

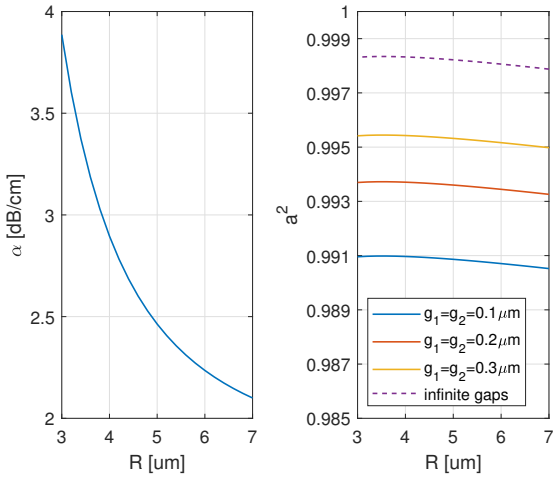

Figure 3. (a) The bending loss of a bent ridge waveguide as a function of radii at 1310 nm. The ridge waveguide parameters are $w_{wg} = 450$ nm, $h_{wg} = 300$ nm, $h_{slab} = 50$ nm. (b) The MRR round-trip power loss as function of radius. Each curve represents a different gap, where $g_1 = g_2$.

To calculate the extinction ratio for the SIN power penalty at the transmitter-side, the through transfer functions at '0' and '1', denoted as $H(j\omega_c)$ and $\tilde{H}(j\omega_c)$, respectively, are required. $H(j\omega_c)$ is evaluated using the method mentioned previously, and to find $\tilde{H}(j\omega_c)$ we used wafer-level measurements of a collection of MRRs fabricated at a commercial foundry (STMicroelectronics). The measurements include the changes of resonance, group refractive index and the full-width half magnitude (FWHM) as a function of the driving current. The measurements of the shift of resonance $\Delta\lambda_r$ versus the driving current I_D for a MRR with $R = 5\mu$m and $g_1 = g_2 = 150$ nm are shown in Fig. 4(a), where the dot marker represents the measurements. Similar trends are observed for rings with other gap values. The shift of resonance as function of the driving current can be described as [18]:

$$\Delta\lambda_r = -\hat{a}\left(\sqrt{1+\frac{I_D}{I_0}}-1\right)+\hat{c}\cdot I_D^2, \tag{4}$$

where $\hat{a}$, I_0, $\hat{c}$ are the fitting coefficients obtained from our measurements. In the case of $R = 5$ μm the fitting coefficients are $\hat{a} = 0.1483$, $I_0 = 0.0085$, $\hat{c} = 0.069$. The new resonance is $\tilde{\lambda_r} = \lambda_r + \Delta\lambda_r$, where λ_r is the resonance of '0' symbol.

The applied driving voltage on the p-i-n junction of a carrier-injection ring results in a blue-shift of the resonance, which then results in a higher power attenuation coefficient. Assuming that the loss grows linearly, the loss at the shifted resonance $\tilde{\lambda_r}$ is:

$$\tilde{\alpha} = \hat{\alpha} + \mathcal{C}\cdot\Delta\lambda_r, \tag{5}$$

where $\hat{\alpha}$ is the total power attenuation coefficient at 0 V driving voltage and $\mathcal{C}$ is the fitting coefficient to measurements. The changes in loss can be evaluated from the measurements of the shifted resonance $\Delta\lambda_r$ and shifted FWHM using [27]:

$$\text{FWHM} = \frac{(1-r_1r_2a)\lambda_r^2}{\pi n_g L\sqrt{r_1r_2a}}, \tag{6}$$

where n_g is the group refractive index. It is assumed that the self-coupling coefficients do not change with I_D. The calculated changes in loss are shown in Fig. 4(b). The continuous curve is a linear fitting to the calculated values. It was found that for MRRs with $R = 5$ μm and $g_1 = g_2 = 150$ nm the fitting coefficient is $\mathcal{C} = -13.298$. A similar trend is observed for other gap values.

Given $\tilde{\lambda_r}$ and $\tilde{\alpha}$, the transfer function $|\tilde{H}(j\omega_c)|^2$ can be calculated using temporal coupled mode theory [29]:

$$|\tilde{H}(j\omega_c)|^2 = \frac{\Delta\omega^2+(\gamma-\mu_1^2)^2}{\Delta\omega^2+\gamma^2}, \tag{7}$$

where $\Delta\omega = \omega - \tilde{\omega_c}$, $\gamma = \frac{1}{\tilde{\tau_i}} + \frac{1}{\tau_{c_1}} + \frac{1}{\tau_{c_2}}$, $\tilde{\tau_i} = \frac{2}{\nu_g\tilde{\alpha}} = \frac{2n_g}{c\cdot\tilde{\alpha}}$ is the intrinsic time constant at $\tilde{\lambda_r}$, $\tau_{c_i} = \frac{2}{\mu_i^2}$ is the coupling time constant, $\mu_i^2 = (1-r_i^2)\cdot\Delta f_{\text{FSR}}$ is the field coupling coefficient, $\Delta f_{\text{FSR}} = \frac{c}{n_g\cdot L}$ is the free spectral range (FSR) in term of frequency, and $i = 1, 2$.

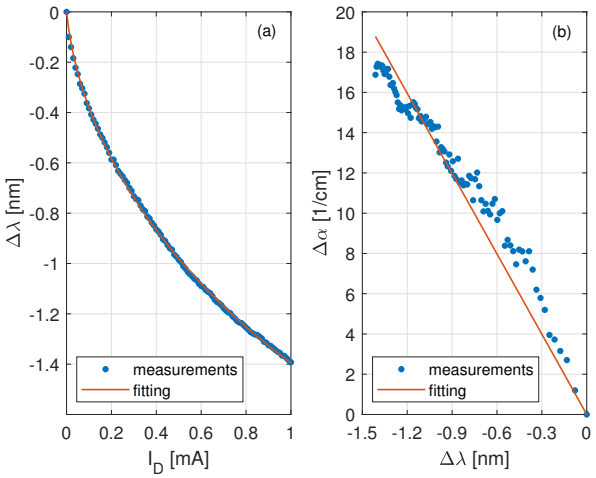

Figure 4. (a) The measured (dot) shift of resonance as a function of the driving current of MRRs designed for a 1305 nm resonance band. The continuous line is the fitted curve to the measurements. (b) The loss coefficient as function of the shift of resonance. The dots represent the calculation from measurements of FWHM, and the continuous curve stands for linear fitting. In both, the MRR parameters are $R = 5$ μm, $g_1 = g_2 = 150$ nm, $w_{bus} = 330$ nm, $w_{ring} = 450$ nm, $h_{wg} = 300$ nm, $h_{slab} = 50$ nm.

D. Receiver sensitivity

In the considered link architecture, each of the DWDM channels is converted to an electrical signal by a PD followed by a trans-impedance amplifier (TIA). For a given link configuration, the increase in the signal data rate results in increases of the power penalties [19] and consequently lower EROP at the input of the PD. Therefore, to increase the aggregated data rate, it is crucial to use a PD with a high sensitivity such that the power margin of the link is maximized for a given link configuration. Avalanche photodiodes (APDs) are known for their high sensitivity [30]. However, APDs can have significant power penalty enhancement due to the relative intensity noise (RIN) of the laser (the measured RIN of the Innolume comb laser is $-135\frac{\text{dB}}{\text{Hz}}$), a limited integration with CMOS-based

drivers [31], and a high bias. On the other hand, germanium-based p-i-n PDs can operate under low-bias which results in a lower power consumption [31]. Germanium (Ge) is considered to be a promising choice for light detection in the wavelength range of optical communication due to its excellent absorption region, good crystalline quality, and integration scheme that utilizes the Si-CMOS process and tools at a low cost [32]. Therefore, in our analysis, we consider germanium-based p-i-n PDs. In Ref. [33], a SiP receiver is reported consisting of a vertical-illumination type Ge-on-Si PD hybrid-integrated with a 65 nm bulk CMOS receiver front-end circuit. The receiver module exhibits high sensitivity performance up to 36 Gbps at 1550 nm, where a sensitivity of -11 dBm was measured for 25 Gbps at a BER of 10^{-12}. Alternatively, in Ref. [31] the potential of lateral p-i-n Ge PDs integrated with Si waveguides is studied. The work predicts the sensitivity to be -15.4 and -14 dBm at 1550 nm for data rates of 25 and 40 Gbps, respectively, for a BER of 10^{-12}. However, in practical devices the sensitivity is worse than the idealized case. In Ref. [32], the design and fabrication of a p-i-n waveguide PD made of a lateral hetero-structured Si-Ge-Si is described, and a bandwidth of 30 GHz at 1550 nm under reverse bias of -3 V and a dark current lower than 150 nA were measured. Also, the reported device achieved a sensitivity at 25 Gbps of -11.25 dBm for a BER of 10^{-9}. From the sensitivity trend of 25 Gbps, one can estimate the sensitivity for this lateral PD as -10.5 dBm for a BER of 10^{-12}. The difference between the predicted and measured sensitivities in Refs. [31] and [32], respectively, can be explained by a higher dark current that decreases the actual sensitivity in the practical device. The device dark current introduced by Ge can be controlled by proper design of the device thickness and p-i-n junction area. In the link budget analysis we will use the measurement results reported in [33], [32] to evaluate the maximum data rate that can be achieved with current technology, and predict the potential data rate of a ring-based SiP link using a PD with sensitivity as in [31]. In our analysis, we assumed the sensitivity in the O-band of the PDs in Refs. [31], [32], [33] is similar to the reported sensitivity in the C-band.

E. Link budget analysis

In this section, we describe the methodology to find the link configuration that maximizes the aggregated data rate. Given the fixed channel spacing (0.28 nm) of the analyzed Innolume comb laser, increasing the channel count is the only way on the light source side to increase the aggregated data rate. From Fig. 2, the maximum consecutive channel count is 24. For this channel count, a supply current of 261 mA minimizes the laser power consumption per channel. The aggregated data rate can also be increased if the power penalties of the cascaded ring modulators and filters are minimized for a channel-specific data rate. Here, we studied the impact of the gap on the power penalties, where we assumed $g_1 = g_2$ for simplicity. At the transmitter-side, a high quality factor is desired to reduce the crosstalk and improve the extinction ratio (ER) such that the SIN power penalty reduced as well. This can be achieved by increasing the gaps g_1 and g_2. However, ring-based modulators with high quality factors are more sensitive to fabrication and temperature fluctuations such that out of tuning is more likely. Therefore, we considered various gaps of the ring-based modulator g_{TX} with the aim to minimize the power penalty at the transmitter-side. We limited the gap scanning to a maximum quality factor of 25,000. This translates to a maximum gap of 180 nm for a ridge waveguide MRR with $R = 5$ μm, $w_{ring} = 450$ nm, $w_{bus} = 330$ nm, $h_{wg} = 300$ nm, $h_{slab} = 50$ nm. To ensure an adequate ER value, we set the wavelength difference between '0' and '1' to $\Delta\lambda_r = \mathcal{A} \cdot \text{FWHM}$, where $\mathcal{A}$ is a positive real number. In our analysis we set $\mathcal{A} = 1$, which provides a sufficiently large ER value. Additionally, from the measurements in Ref. [22], the average refractive index of this ridge waveguide MRR is $n_g = 4.12$, which leads to FSR of $13.26\,\text{nm}$ at 1310 nm. Given that the channel count is 24 with channel spacing of 0.28 nm, the DWDM wavelength range is approximately 6.44 nm, which is lower than the FSR of the analyzed rings.

At the receiver-side, the power penalties depend on the filter shape, i.e., IL at resonance, bandwidth, and rejection. Therefore, it is useful to plot the design space of the MRR. One can define the design space to be IL better than 1 dB, bandwidth range of 10-50 GHz (to support channel data rates of 10-50 Gbps), and rejection better than 30 dB. We plotted the design space of ring-based filter for identical and non-identical ring-bus ridge waveguide widths, using the performance terms in [27] together with the behavioral bus-ring coupling model proposed in [28] and the round-trip loss model in Eq. (3). The design space performances are shown in Fig. 5(a)-(c) and Fig. 6(a)-(c) for identical and non-identical bus-ring widths, respectively. The white area is the desired design space of each of the performance parameters. Combining all the three design spaces leads to Figs. 5(d) and 6(d). It is important to note that the design space of a ring-based filter with narrow bus has larger gap values, where most of the design gap values are above 100 nm, which is the minimum standard gap value for fabrication.

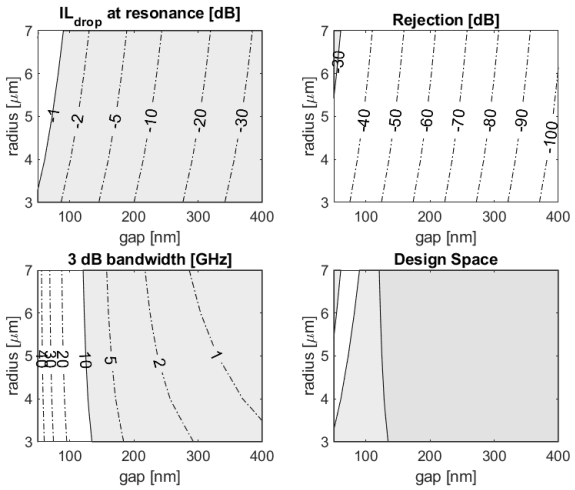

Figure 5. Performance contours and design space of MRR with identical bus-ring widths at 1310 nm. $w_{bus} = 450$ nm, $w_{ring} = 450$ nm, $h_{wg} = 300$ nm, $h_{slab} = 50$ nm. The white area is the desired design space. (a) IL at resonance. (b) Rejection. (c) Bandwidth. (d) The design space considering all three performance parameters.

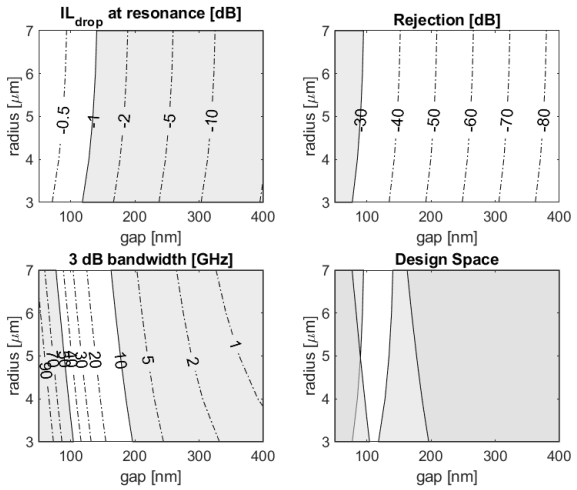

Figure 6. Performance contours and design space of MRR with non-identical bus-ring widths at 1310 nm. $w_{bus} = 330$ nm, $w_{ring} = 450$ nm, $h_{wg} = 300$ nm, $h_{slab} = 50$ nm. The white area is the desired design space. (a) IL at resonance. (b) Rejection. (c) Bandwidth. (d) The design space considering all three performance parameters. The design space of MRR with narrow bus has larger gap values compared to MRR with identical ring-bus widths. This results in a less sensitive design for fabrication variations.

Figs. 5 and 6 provide insights on the desired design space to achieve the specification requirements of a single ring-based filter, but not if the power budget is enough to close the loop, i.e., the EROP of all the NRZ-OOK DWDM channels is above the sensitivity, taking into account the interaction between the photonic components. Therefore, to evaluate the EROP of NRZ-OOK DWDM signals at the PD input we scanned the gaps of the ring-based filter g_{RX}, in addition to the gap scanning of the ring-based modulator, to minimize the power penalty at the receiver-side for a given data rate. We limit the gap scanning such that the minimum 3 dB bandwidth of the filter will be slightly higher than the channel data rate to avoid severe inter-symbol interference (ISI). In our analysis, we have considered a ridge waveguide MRR with $R = 5$ μm, $w_{ring} = 450$ nm, $w_{bus} = 330$ nm, $h_{wg} = 300$ nm, $h_{slab} = 50$ nm. At each channel data rate, R_b, and gap values of the ring-based modulator and filter, g_{TX} and g_{RX}, we estimated the worst EROP: $\psi = \min\{\text{EROP}(R_b, g_{TX}, g_{RX})\}$. Fig. 7 shows ψ as a function of g_{TX} for various R_b values, where each curve represents a different g_{RX} value. Let $\hat{g}_{TX}^{R_b}$ and $\hat{g}_{RX}^{R_b}$ represent the optimal values that maximize ψ for a data rate R_b, respectively. Fig. 8(a) shows $\psi(\hat{g}_{RX}^{R_b})$ as a function of g_{TX}, where each curve stands for different R_b value. Hence, $\hat{g}_{TX}^{R_b}$ can be defined as the maxima of $\psi(\hat{g}_{RX}^{R_b})$. Fig. 8(b) presents a comparison between $\psi(\hat{g}_{TX}^{R_b}, \hat{g}_{RX}^{R_b})$ and the receiver sensitivity, PD_{sen}, reported in [31], [32], [33], where the sensitivity of Ref. [32] was estimated for BER of 10^{-12}. The maximum channel data rate is the intersection between $\psi(\hat{g}_{TX}^{R_b}, \hat{g}_{RX}^{R_b})$ and PD_{sen}. Another useful insight from Figs. 7 and 8(a) is on the performance sensitivity to fabrication variations of g_{TX} and g_{RX}. Fig. 7 shows that variations in g_{RX} result in significant performance changes of ψ for data rates higher than 15 Gbps. On the other hand, as can be observed from Fig. 8(a), variations in g_{TX} result in small performance changes around the maxima of ψ.

For the receiver sensitivities in Refs. [31], [32] the maximum NRZ-OOK channel data rate is 20 and 22 Gbps, respectively, which leads to aggregated data rates of 480 and 528 Gbps. The aggregated data rate of the analyzed link can be as high as 660 Gbps if the predicted receiver sensitivity in Ref. [33] is considered. Considering the next generation of transceivers will support 1 Tbps and higher, further increases of the comb output power and reduction of the link losses and power penalties are required. In the case of quantum dot-based combs, optimizing mirror reflectivities, number of layers, confinement factor, and device length are anticipated to boost the optical power by a few dB. Furthermore, improving the comb light coupling to the SiP chip will enable a lower comb power budget threshold (currently $\mathcal{P}_b = 0$ dBm) and as a result, additional comb lines might be available. Moreover, increasing the spacing between the comb lines (currently 0.28 nm) can reduce the crosstalk penalty, which is expected to increase the available link budget. In these design improvement suggestions, the SiP device performance, such as the FSR of the rings and the bandwidth of the GCs, might limit the scaling of the data rate and in turn require other techniques to be considered, such as outskirt DWDM channels with lower data rates. Other options to scale up the aggregated data rate, such as high-order modulation formats and dual-polarization multiplexing, should be carefully considered as the initial eye opening and the available optical power are lower.

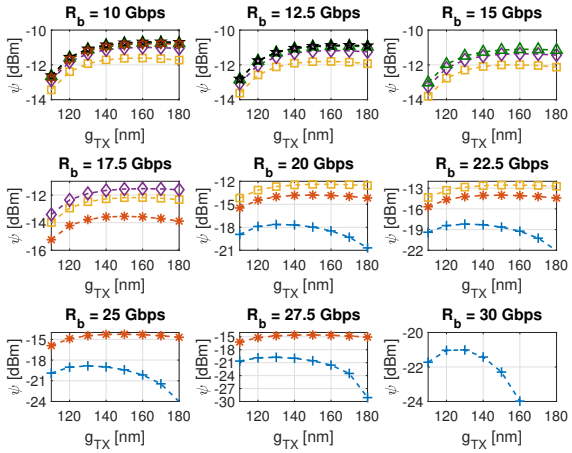

Figure 7. ψ as a function of g_{TX} for various R_b values. Each curve stands for different g_{RX} value: 110 nm (blue-cross), 120 nm (red-asterisk), 130 nm (yellow-square), 140 nm (purple-diamond), 150 nm (green-triangle), 160 nm (black-pentagram) or 170 nm (brown-hexagram).

III. Power Consumption: Models and Analysis

In this section the energy consumption of the analyzed comb source ring-based SiP link is estimated at the maximum aggregated data rate. The energy consumption analysis includes the comb source, Serializer/Deserializer (SerDes), driver, thermal tuning and the TIA. From Fig. 2, the power consumption of the laser at supply current of 261 mA is 0.476 W. The models and power consumption of the other transceiver elements that we have been using in our analysis are described below.

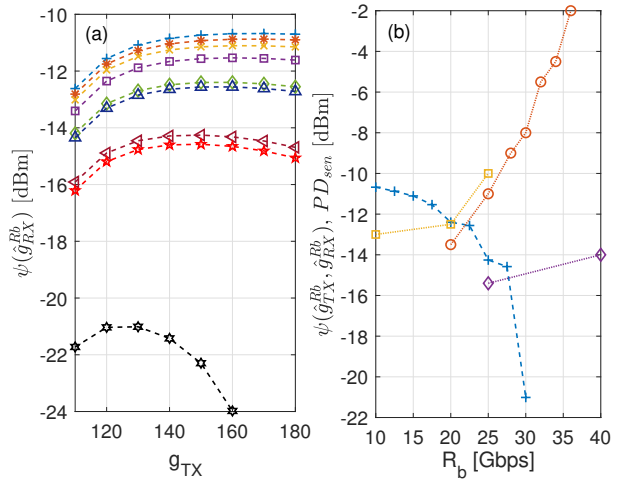

Figure 8. (a) $\psi(\hat{g}_{RX}^{R_b})$ as a function of g_{TX}. Each curve stands for different $\hat{g}_{RX}^{R_b}$: $\hat{g}_{RX}^{10\text{ Gbps}} = 160$ nm (blue-cross), $\hat{g}_{RX}^{12.5\text{ Gbps}} = 160$ nm (red-asterisk), $\hat{g}_{RX}^{15\text{ Gbps}} = 150$ nm (yellow-oblique cross), $\hat{g}_{RX}^{17.5\text{ Gbps}} = 140$ nm (purple-square), $\hat{g}_{RX}^{20\text{ Gbps}} = 130$ nm (green-diamond), $\hat{g}_{RX}^{22.5\text{ Gbps}} = 130$ nm (blue-triangle), $\hat{g}_{RX}^{25\text{ Gbps}} = 120$ nm (purple-rotated triangle), $\hat{g}_{RX}^{27.5\text{ Gbps}} = 120$ nm (red-pentagram), $\hat{g}_{RX}^{30\text{ Gbps}} = 110$ nm (black-hexagram). (b) $\psi(\hat{g}_{TX}^{R_b}, \hat{g}_{RX}^{R_b})$ as a function of the data rate (blue-cross) compared to the receiver sensitivity reported in Refs. [31], [32], [33] (purple-diamond, yellow-square, red-circle, respectively). The maximum channel data rate is at the intersection point between $\psi(\hat{g}_{TX}^{R_b}, \hat{g}_{RX}^{R_b})$ and PD_{sen}.

A. SerDes

The increase in demand for processing and memory resources by data-intensive applications necessitates serializer/deserializer (SerDes) transceivers to compensate for limited input/output computing components, i.e., CPU, GPU and memory. In this work, we do not consider the energy consumed by the SerDes as a contributing source to the energy per bit metric of the link since the SerDes is typically considered to be part of the compute node rather than the interconnect. However, we briefly note the relative energy consumption of the SerDes here to illustrate its contribution to the full system. The wide bandwidth needed to be supported, the timing requirement for the data and clock alignment in the transmitter make the realization of high-speed NRZ SerDes transceiver challenging, resulting in significant power consumption [34]. In Refs. [35], [34], [36], NRZ SerDes transceivers in CMOS technologies exhibit energy consumption of 10.9-14.7 $\frac{\text{pJ}}{bit}$ for data rates of 16-56 Gbps.

B. Driver

Carrier-injection rings are limited by their response time. To improve the response time of the ring, the driver is designed with a pre-emphasis stage. A high-level block diagram of the driver with 1-tap pre-emphasis stage is shown in Fig. 9. The driver consists of two cross-coupled drivers that have different driving strengths. Let us assume that the gain of the main driver is normalized to 1, the gain of the pre-emphasis driver is α, and the input of the pre-emphasis driver stage is delayed by τ, where τ is a fraction of unit interval (UI). This results in four different voltage levels, i.e., $1 \pm \alpha$ and $-1 \pm \alpha$, depending on the data. Thus, the pre-emphasis amplitude gain is $\frac{1+\alpha}{1-\alpha}$. The pre-emphasis gain increases as the strength of the pre-emphasis driver gets closer to the main driver stage, and is ideally infinite when $\alpha = 1$.

The driver with a 1-tap pre-emphasis stage can be implemented using inverters. In this case, the strength of each driver stage can be represented by the turn-on impedances as illustrated in Fig. 10. It is assumed that the turn-on impedances of the NMOS and PMOS of the inverters are identical: R_M for the main driver, and R_P for the pre-emphasis driver. In this implementation, the maximum voltage level, $1+\alpha$, corresponds to the supply voltage, V_{DD}, and the minimum voltage level, $1-\alpha$, corresponds to the ground voltage, $V_{\text{SS}} = 0$. At the rising and falling times of the data, both drivers have the same polarity, such that only negligible amount of dynamic current flows. Then for τ moments, the output voltage level is V_{DD} or 0 depending on the data, and there is no power consumption during this time. After τ moments, the main and the pre-emphasis drivers have the same polarity, such that they compete and generate a static voltage level of $V_{\text{DD}}\frac{R_M}{R_M+R_P}$ or $V_{\text{DD}}\frac{R_P}{R_M+R_P}$ depending on the data. During this period of time, a static current of $I_{\text{DC}} = \frac{V_{\text{DD}}}{R_M+R_P}$ flows from V_{DD} to V_{SS}. This generates a static power of $P_{\text{DC}} = V_{\text{DD}} \cdot I_{\text{DC}}$, which is the dominant power consumer in this driver design. Therefore, the total power consumption of the driver can be estimated by:

$$P_{\text{D}} = Pr(X = 0) \cdot P_{\text{DC}} + Pr(X = 1) \cdot (1 - \tau) P_{\text{DC}}, \quad (8)$$

where $Pr(X = k)$ is the transmission probability of a $k \in \{0, 1\}$ on-off keying (OOK) symbol. In the case of equal transmission probability, Eq. (8) simplifies to $P_{\text{D}} = (1 - \frac{\tau}{2})P_{\text{DC}}$. It should be noted that for channel data rate of ~20 Gbps and higher two cascaded drivers are needed, which doubles the power consumption of the driver. In the power consumption analysis we assumed, $\tau = 0.5 \cdot \text{UI}$, $V_{\text{DD}} = 0.9$ V (28 nm platform), and $R_M + R_P = 100\ \Omega$, which results in driver power consumption of 15 mW for data rates higher than 20 Gbps. The estimated area of the driver device (28 nm platform), which includes the pre-driver with variable delay, pre-emphasis driver, bump pads, and additional on-chip peripheral circuitry, is 65 $\times$ 120 μm^2.

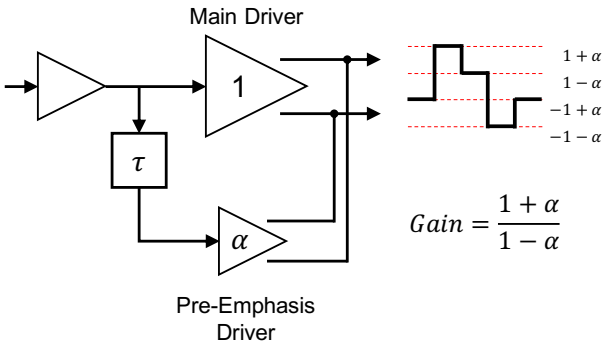

Figure 9. A 1-tap pre-emphasis driver block diagram.

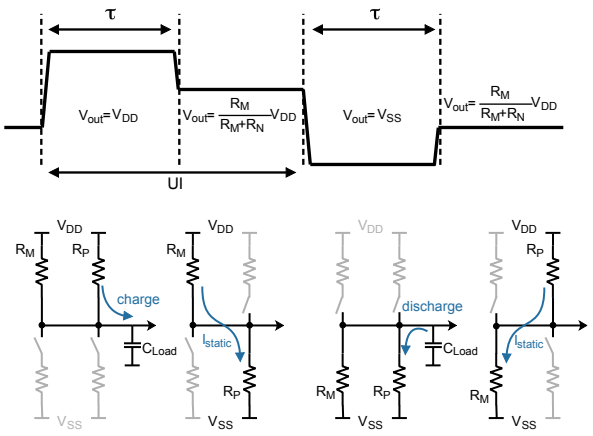

Figure 10. Turn-on states of the driver.

C. MRR heater

The optical behavior of SiP devices is very sensitive to the environmental temperature due to the strong thermo-optic coefficient of silicon [37]. Specifically, the resonance of MRR SiP devices can shift during operation due to environmental temperature fluctuations. Therefore, MRR SiP devices consist of heating elements controlled by thermal rectification algorithms to stabilize the temperature in the ring area [38], [39]. However, the thermo-optic effect of silicon can also be an opportunity to compensate for fabrication variations. The resonance of fabricated MRR devices can be out of tune from the desired wavelength. Thus, at the beginning of operation the ring area is heated to tune the resonance to the desired wavelength. In the following power consumption analysis we assumed that the required power for resonance tuning at the beginning of operation is significantly higher than the required power for the temperature stabilization during operation.

Common designs of the heating elements use metal- or doped silicon-based heaters. The quality of the heater is determined by its efficiency, typically given in $\frac{\text{mW}}{\text{nm}}$ or $\frac{\text{mW}}{\text{FSR}}$ dimensions. The latter is considered to be a more universal metric across different ring radii [40]. Metal heaters are placed on top of the MRR to directly heat the silicon waveguide of the ring. However, a separation between the metal heater and the ring resonator, on the order of 1 μm, is required to preserve the desirable optical mode of the silicon waveguide [41]. As a result, the tuning efficiency is limited and lower than ideal. Metal heaters with multi-wire structures are used to improve the tuning efficiency. Refs. [42] and [43] report titanium (Ti) heaters with tuning efficiencies as high as 105 and ~42 $\frac{\text{mW}}{\text{FSR}}$ (6.187 and 2.625 $\frac{\text{mW}}{\text{nm}}$) in the C-band, respectively. Ω-shaped Ti heaters, which follow the ring structure and are designed for uniform yet contained heat distribution, achieved a tuning efficiency of 35.2 $\frac{\text{mW}}{\text{FSR}}$ (4 $\frac{\text{mW}}{\text{nm}}$; C-band) [44]. Further improvement in the tuning efficiency performance can be achieved by using thermal isolation trenches and undercuts around and below the ring silicon waveguide. Ref. [45] reports a tuning efficiency of 21 $\frac{\text{mW}}{\text{FSR}}$ (1.10 $\frac{\text{mW}}{\text{nm}}$; C-band) with the use of isolation trenches. Significant enhancement in the tuning efficiency performance of 2.4 $\frac{\text{mW}}{\text{FSR}}$ (0.2-0.37 $\frac{\text{mW}}{\text{nm}}$; C-band) is described in [46] for a Ti heater with thermal isolation trenches and undercuts. However, the etch removal of the substrate may reduce the yield of the SiP process, making this technique unsuitable for current commercial production lines [41]. On the other hand, doped heaters, which are integrated within the silicon MRR, provide direct and efficient tuning due to the lower heat capacity and reduced thermal conductance compared to metal heaters [47]. However, the integrated heater should be carefully placed to minimize its interference with the optical mode [41]. In Ref. [48], it is proposed to use adiabatic resonant microrings (ARMs), which enable direct integration of the heater element within the resonator due to the suppression of the higher-order modes to achieve efficient tuning, resulting in a tuning efficiency of 24.5 $\frac{\text{mW}}{\text{FSR}}$ (0.54 $\frac{\text{mW}}{\text{nm}}$; C-band). Similarly, the confinement of the TE mode at the outer edge of the ring waveguide allows placement of directly contacted doped heaters at its inner edge [47]. The inner periphery of the MRRs is doped in patches to increase the heater resistance. The reported tuning efficiency is 20 $\frac{\text{mW}}{\text{FSR}}$ (0.57 $\frac{\text{mW}}{\text{nm}}$; C-band). Furthermore, in Ref. [49], a resistive microheater, which is placed within the cavity of a ring modulator that is fabricated in a state-of-the-art CMOS process, has a tuning efficiency of 10.625 $\frac{\text{mW}}{\text{FSR}}$ (0.625 $\frac{\text{mW}}{\text{nm}}$; O-band). Additional improvements in this microheater design achieved a tuning efficiency of 6.22 $\frac{\text{mW}}{\text{FSR}}$ (0.37 $\frac{\text{mW}}{\text{nm}}$; O-band) [50]. Substrate removal is used in the fabrication of the ring modulators in Refs. [49], [50], which can explain the high tuning efficiency. However, this is an advanced fabrication technique, which is not currently supported in most standard SiP platforms. In this work, the MRRs have been designed with doped heaters. At the beginning of operation, the maximum detuning of the rings is one FSR. We assumed that the tuning efficiency is approximately identical for the O- and C-bands. To be conservative in our analysis, we used tuning power of the doped heaters reported in Refs. [47] (20 $\frac{\text{mW}}{\text{FSR}}$).

D. Trans-impedance amplifier

A library of various trans-impedance amplifier (TIA) designs in 65 nm and 28 nm platforms taken from [51], is used in this work. Each of the TIAs is the most energy efficient design at a given data rate R_b and input current I_{TIA}. Using the database, the TIA energy consumption per bit versus the input current is shown in Fig. 11(a) and (b) for 65 nm and 28 nm platforms, respectively. Each marker represents a different data rate. In both platforms, the energy consumption at a specific data rate decreases as the input current increases. This can be explained by the parasitic capacitance of the MOS transistors affected by the incoming high speed signal (tens of Gbps), which leads to the generation of a feedforward path from the input to the output of the TIA. This feedforward path current contributes to charging of the output capacitance load such that less supply current is needed to build up the required voltage on the load. The energy consumption versus the data rate is shown in Fig. 12(a) and (b) for 65 nm and 28 nm platforms, respectively. Each of the dots represents the energy consumption as a function of data rate and TIA input current. The TIA input current I_{TIA} is scanned in the range of 1 μA

- 249 μA. However, at a given data rate, a design might be available only from a minimum TIA input current, i.e., $I_{\text{TIA,min}}(R_b) > \min(I_{\text{TIA}})$. The blue crossbar stands for the energy consumption at $I_{\text{TIA,min}}(R_b)$, and the Pareto front of the minimum E_b is marked by the red dots. It can be observed that at minimum TIA input current, the power consumption is higher than the Pareto front, where it is more noticeable for 65 nm platform. The power budget analysis in section II-E shows that the LROP of the optimal gap settings at $R_b = 20$ Gbps is -12.4 dBm. This results in $I_{\text{TIA}} < 50$ μA for a PD responsivity of 0.75 $\frac{A}{W}$ [31], [33], which is lower than $I_{\text{TIA,min}}$ at $R_b = 20$ Gbps of 65 nm platform. Therefore, in the power consumption analysis we considered the 28 nm platform.

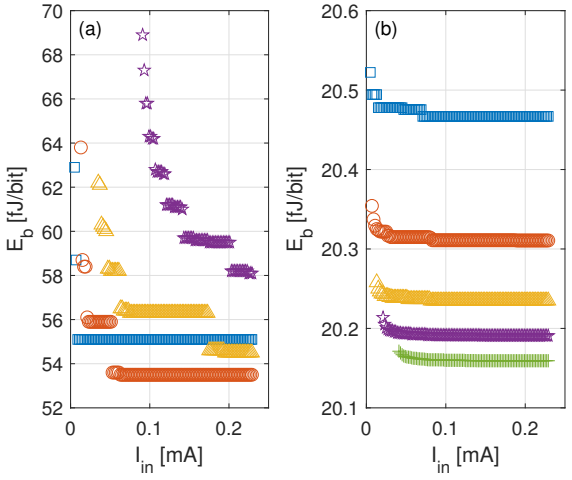

Figure 11. Energy consumption per bit versus TIA input current for data rates of 10 Gbps (rectangular), 15 Gbps (circle), 20 Gbps (triangle), 25 Gbps (pentagram), and 30 Gbps (crossbar). (a) 65 nm platform. (b) 28 nm platform.

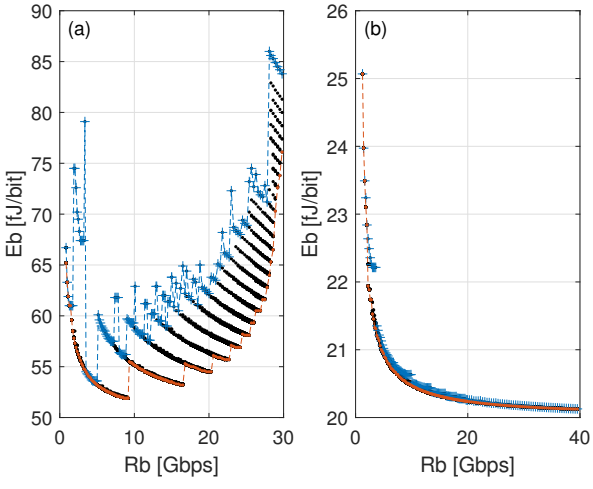

Figure 12. Energy consumption per bit versus data rate. (a) 65 nm platform. (b) 28 nm platform. Each of the dots represents a different TIA input current, and the crossbar marker stands for the energy consumption at $I_{\text{TIA},min}(R_b)$. The Pareto front of the minimum E_b is marked by the red dots. It can be observed that at $I_{\text{TIA},min}(R_b)$, the power consumption is higher than the Pareto front.

E. Energy analysis

In section II-E, we found that the maximum channel data rate is 22 Gbps for the PD in Ref. [33]. If the predicted receiver sensitivity in Ref. [31] is considered, the channel data rate can be as high as 27.5 Gbps. Let $E_b^{R_b}$ represent the energy consumption of a device in the analyzed link at a specific data rate. Table I summarizes the energy consumption of each of the link devices at channel data rates of 12.5 Gbps, 22 Gbps and 27.5 Gbps. It is shown that the energy consumption of the analyzed comb source ring-based SiP link can be as low as 2.64 $\frac{\text{pJ}}{\text{bit}}$ with an aggregated data rate of 660 Gbps. In Fig. 13, the relative share of the overall energy consumption of each component in the analyzed link for data rates of 22 Gbps and 27.5 Gbps is shown. To achieve link energy consumption below 1 $\frac{\text{pJ}}{\text{bit}}$, further improvements in power consumption of the SiP link devices are required—mainly the heaters, and to a lesser degree, the comb source and drivers. Given the power consumption of advanced metal heaters (2.4 $\frac{\text{mW}}{\text{FSR}}$ [46]), the power consumption of the heaters (TX and RX) can be reduced to 0.18 $\frac{\text{pJ}}{\text{bit}}$ at a channel data rate of 27.5 Gbps. Additionally, assuming better utilization of the comb source, e.g., higher count of available lines such that 1 Tbps is supported (improvement factor of 1.52), while keeping the same power consumption, the energy consumption of the comb can be reduced to 0.475 $\frac{\text{pJ}}{\text{bit}}$. This leads to a total link power consumption of 1.115 $\frac{\text{pJ}}{\text{bit}}$, which presents an improvement in the energy efficiency of current SiP links and approaches the roadmap energy efficiencies proposed for the 2025 era[2,3].

Table I
THE ENERGY CONSUMPTION OF THE LINK DEVICES FOR 24 CONSECUTIVE COMB LINES AND SELECTED DATA RATES.

Device	$E_b^{12.5\text{ Gbps}}$ [pJ/bit]	$E_b^{22\text{ Gbps}}$ [pJ/bit]	$E_b^{27.5\text{ Gbps}}$ [pJ/bit]
Comb laser	1.59	0.9	0.72
Driver	0.49	0.54	0.44
Heater (TX and RX)	3.2	1.82	1.46
TIA	0.02	0.02	0.02
Total	**5.3**	**3.28**	**2.64**

IV. CONCLUSIONS

In this work, we analyzed a ring-based NRZ-OOK SiP link architecture with a commercially available comb laser source. We proposed a new figure of merit, the EWPE, to find the most energy efficient comb laser settings at a specific channel count and power budget. Additionally, we considered MRRs with narrow bus waveguides, which have a design space with larger gap values compared to MRRs with identical ring-bus widths. This results in a design less sensitive to fabrication variations. By leveraging known power penalty models supported by

[2]DARPA Photonics in the Package for Extreme Scalability (PIPES); https://www.darpa.mil/news-events/photonics-in-the-package-for-extreme-scalability-proposers-day

[3]ARPA-E ENergy-efficient Light-wave Integrated Technology Enabling Networks that Enhance Datacenters (ENLITENED); https://arpa-e.energy.gov/?q=arpa-e-programs/enlitened

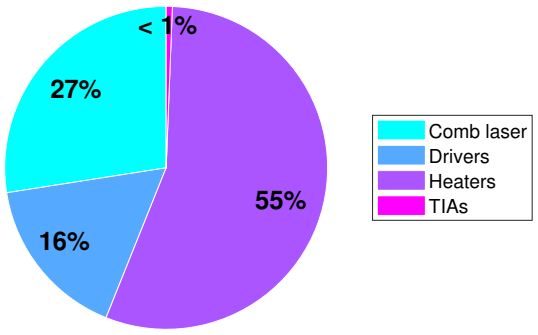

Figure 13. The relative share of overall energy consumption of each component in the analyzed link for data rates of 22 Gbps and 27.5 Gbps.

comb laser and MRR measurements, we estimate the EROP at the receiver input of each of the DWDM channels. For a link architecture with 24 consecutive comb lines, we found that the channel data rate can be up to $R_b = 22$ Gbps, which is higher than reported in other works such as Ref. [52], due to lower power penalties. In the case of an improved receiver design with lower parasitics, as predicted in Ref. [31], the channel data rate can be as high as 27.5 Gbps. While carrier-injection ring-based modulators have a higher modulation efficiency, they require a more complex driver design to compensate for the slow response time. However, the power consumption is mainly static such that the energy per bit metric decreases as the data rate increases (at ~20 Gbps and above the energy per bit is doubled due to the need to use dual cascaded drivers). Considering the maximum aggregated data rate of 528 Gbps (projected 660 Gbps) encoded into a single-polarization, the energy consumption of the optical transceiver including the comb laser, drivers, heaters and TIAs is 3.28 $\frac{\text{pJ}}{\text{bit}}$ (projected 2.64 $\frac{\text{pJ}}{\text{bit}}$). Our link analysis, which is supported by comb laser and MRR measurements, is an important step towards transceivers with data rates of 1 Tbps. The proposed ring-based OOK SiP link is expected to support this data rate with further reduction of the losses and power penalties. This can increase the available channel count, link budget and data rate per channel, such that the transceiver data rate scales up toward 1 Tbps.

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Yanir London received his Ph.D. degree in electrical and computer engineering from Ben–Gurion University of the Negev, Beer-Sheva, Israel, in 2017. He is currently a Postdoctoral Research Scientist at the Lightwave Research Laboratory, Columbia University, New York, NY, USA. His current research interests include silicon photonics devices, efficient interconnections for high performance computing, and digital signal processing algorithms for optical communication systems.

Thomas Van Vaerenbergh received his master degree in applied physics and his Ph.D. degree in photonics from Ghent University, Belgium, in 2010 and 2014, respectively. Since 2014 he has been working in Hewlett Packard Labs, Palo Alto, CA. His main research interests are optical computing, accelerators for combinatorial optimization, and the modeling and design of passive silicon photonic devices such as microring resonators and grating couplers.

Anthony J. Rizzo received his B.S. degree in physics from Haverford College, Haverford, PA in 2017 and his M.S. degree in electrical engineering from Columbia University, New York, NY in 2019. He is currently working toward his Ph.D. degree in the Lightwave Research Laboratory at Columbia University under Professor Keren Bergman, with research interests in silicon photonic devices and systems for high performance computing and quantum information science applications.

Peng Sun received the Ph.D. degree in electrical engineering from the Ohio State University, Columbus, OH in 2012. He was a senior engineer at Luxtera Inc., Carlsbad, CA from 2012 to 2018. He is currently a research engineer at Hewlett Packard Labs, Palo Alto, CA.

Jared Hulme received his Ph.D. degree in electrical engineering from University of California, Santa Barbara, CA in 2016. He is currently a silicon photonic engineer at Hewlett Packard Labs, Palo Alto, CA.

Geza Kurczveil is a research scientist in HPE's Systems Architecture Lab in Santa Barbara, California. He received his Ph.D. degree in Electrical and Computer Engineering from the University of California, Santa Barbara in 2012 working on optical buffers. His current research interests include silicon photonic integrated circuits and nano-photonics. He has authored and coauthored over 50 journal and conference papers.

Ashkan Seyedi received a dual Bachelor's in Electrical and Computer Engineering from the University of Missouri-Columbia and a Ph.D. from University of Southern California working on photonic crystal devices, high-speed nanowire photodetectors, efficient white LEDs and solar cells. While at Hewlett Packard Enterprise as a research scientist, he has been working on developing high-bandwidth, efficient optical interconnects for exascale and high performance computing applications.

Binhao Wang (M'16) received the B.S. degree in electrical engineering and the M.S. degree in optical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, and the Ph.D. degree in electrical engineering from Texas AM University, College Station, TX, USA, in 2016. He is a Research Scientist with the Systems Architecture Laboratory in Hewlett Packard Laboratories, Hewlett Packard Enterprise, Palo Alto, USA. He has published 40 peer-reviewed journal and conference papers. His research interests include VCSEL photonics and silicon photonics.

Xiaoge Zeng received the B.Sc. degree in physics from the University of Science and Technology of China, Hefei, Anhui, China, in 2008 and the Ph.D. degree in physics from the University of Colorado Boulder , Boulder, CA, USA in 2015. He has been a research scientist at the Hewlett Packard Labs since 2016. His research interests include silicon photonics, integrated optics, optical communications, nonlinear and quantum optics.

Zhihong Huang is a research scientist at Hewlett Packard Labs, leading the development of low power optical transceivers for optical interconnects. Her research topics include avalanche photodiodes, single photon counting, optical sensors, nano-photonics, silicon photonics, as well as quantum information processing. She has obtained her B.S. degree from Peking University, and her M.S. and Ph.D. degrees in Electrical Engineering from the University of Texas at Austin. She has authored and coauthored over 70 journal and conference papers, and was granted over 20 US/international patents with another dozen pending.

Jinsoo Rhim received the B.S. and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2009 and 2016, respectively. His doctoral dissertation concerned modeling, design, and optimization of Si photonic transmitters. In 2016, he joined Hewlett Packard Laboratories, Palo Alto, USA. His research interests include photonic device characterization and modeling and high-speed ASIC design in advanced CMOS/BiCMOS technology.

Marco Fiorentino is a Distinguished Technologist in the Systems Architecture Laboratory at HPE Labs in Palo Alto, California. He received a Ph.D. in Physics from the University of Napoli, Italy in 2000 working on quantum optics. Before joining HPE Labs, in 2005 he worked at Northwestern University, University of Rome, and MIT. In the past he has worked on optics, high precision measurements, and optical communications. He has published more than 60 papers in peer-reviewed journals and given numerous contributed and invited talks to international conferences. He is a Senior Member of the Optical Society of America.

Keren Bergman (S'87–M'93–SM'07–F'09) received the B.S. degree from Bucknell University, Lewisburg, PA, in 1988, and the M.S. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, in 1991 and 1994, respectively, all in electrical engineering. Dr. Bergman is currently a Charles Batchelor Professor at Columbia University, New York, NY, where she also directs the Lightwave Research Laboratory. She leads multiple research programs on optical interconnection networks for advanced computing systems, data centers, optical packet switched routers, and chip multiprocessor nanophotonic networks-on-chip. Dr. Bergman is a Fellow of the IEEE and OSA.