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Performance Requirements for Terabit-class Silicon Photonic Links Based on Cascaded Microring Resonators

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***Abstract*—The electrical interconnects in high performance computing (HPC) systems are reaching their bandwidth capacities in supporting data-intensive applications. Currently, communication between compute nodes through these interconnects is the main bottleneck for overall HPC system performance. Optical interconnects based on the emerging silicon photonics (SiP) platform are considered to be a promising replacement to boost the speed of the data transfer with reduced cost and energy consumption compared to electrical interconnects. In this paper, we present a comprehensive analysis of a comb source microring-based SiP link architecture with p-i-n photodetectors. In particular, we direct our focus on improved grating coupler and bus waveguide designs to reduce the link power penalties. Additionally, we map the required performance from the comb laser to provide an aggregated data rate of 1 Tbps under the constraints of free spectral range (FSR) and nonlinearities of the microring resonators (MRRs). We show that a select few comb configurations satisfy these requirements, and energy consumption as low as $3\ \frac{\text{pJ}}{\text{bit}}$ is achievable.**

***Index Terms*—High performance computing, optical interconnections, wavelength division multiplexing, energy efficiency, silicon photonics, integrated photonics, ring resonators.**

I. Introduction

THE recent explosion in data-intensive applications such as machine learning and artificial intelligence has stressed the interconnection bandwidth in high performance computing (HPC) and data center (DC) systems [1], [2]. Roadmaps forecast that this upward trend will continue indefinitely over the foreseeable future [3], [4], forcing a paradigm shift in the interconnects to keep up with the increased demands. Optical interconnects show promise as a replacement for electrical interconnects in future HPC and DC systems [5], [6], [7], boasting potential performance numbers that could accommodate the aforementioned rapid data growth while also driving the energy consumption per bit and the cost per bit downward [8], [9], [10]. Furthermore, silicon photonics (SiP) has emerged as one of the material platforms of choice in optical interconnects due to its compatibility with the same CMOS fabrication tools and processes used in the microelectronics industry.

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In addition to leveraging the existing CMOS infrastructure to drive down cost, the SiP platform affords extremely dense integration due to the large refractive index contrast between silicon and its oxide in silicon-on-insulator (SOI) wafers, with numerous demonstrations having shown thousands of photonic devices operating on a single die [11], [12]. Microring resonators (MRRs), one of the fundamental building blocks in integrated photonics, take advantage of this large index contrast in the SiP platform to achieve dense device integration with demonstrated bend radii on the order of a single wavelength [13]. MRRs have shown great versatility in operation—their applications span the full spectrum of optical communications, including generating [14], modulating [15], filtering [16], detecting [17], and switching [18] light. Furthermore, as cavities, MRRs exhibit high wavelength dependence which can be leveraged to selectively modulate and filter separate wavelength channels in a wavelength-division multiplexed (WDM) link.

MRRs in the SiP platform, owing to their small footprint and potential for high speed operation, are the most promising devices for achieving the bandwidth density metrics proposed for future on-board and co-packaged optical links in HPC and DC systems. MRR modulators require a low drive voltage for operation compared to Mach Zehnder modulators, allowing for more straight forward integration with state of the art CMOS electronics. Due to their high wavelength selectivity, many MRRs can be cascaded on a single bus in a WDM architecture to modulate and filter individual channels without the need for a separate MUX/DEMUX stage (Fig. 1). Such an architecture requires many wavelengths with even spectral spacing on the same bus, which lends well to frequency comb sources such as III-V comb lasers and microresonator-based Kerr combs [19], [20].

This work is an extension of that in Ref. [21], building on the results with a specific focus on the near-term technology improvements necessary to achieve terabit-class silicon photonic links based on MRRs rather than the capabilities of currently available technology as analyzed in the previous work. Previous analyses of integrated photonic links for terabit-class communications have focused on different material platforms such as indium phosphide and have used complex modulation formats such as QPSK and QAM with large-footprint devices such as arrayed waveguide gratings (AWGs) and Mach Zehnder modulators [22]. Other similar analyses in the SiP platform have been limited in providing a path to Terabit operation by restricting the photonic devices to a foundry process design kit (PDK) [23]. We differentiate this work by focusing on high bandwidth density architectures (based on cascaded MRRs)

in the SiP platform with custom devices that achieve ultra-low energy per bit operation using standard non-return to zero on-off keying (NRZ-OOK) modulation. NRZ-OOK is chosen since higher order modulation formats such as coherent and four-level pulse amplitude modulation (PAM4) require additional digital signal processing (DSP) and/or forward error correction (FEC) which add additional energy consumption as well as unacceptable latency overhead in HPC systems.

We begin our analysis with a design space exploration of the link, including novel device improvements in the grating couplers and reduced bus waveguide losses. We then comprehensively analyze the energy consumption of the various link components and provide specific paths to improving the efficiencies of each based on the current state of the art. Finally, we conclude with an outlook on the analyzed link design, including design trade-offs and future directions for device improvements to achieve 1 Tbps operation with an energy efficiency of $\leq 1\,\frac{\text{pJ}}{\text{bit}}$.

II. Design Exploration

In this work, we explore the performance requirements to achieve a 1 Tbps aggregated data rate using a cascaded ring-based SiP DWDM link architecture with a comb laser source. In our analysis, the selected ring-based modulators are injection-type due to their low loss and as a result high quality factor (Q-factor), which provides better scalability of the line count within a single free-spectral range (FSR) compared to depletion-type ring modulators. A block diagram of the link architecture is shown in Fig. 1. The photonic components include the comb laser source, grating couplers, cascaded-ring modulators, cascaded-ring filters and photodetectors (PDs). The electronic devices include the drivers and trans-impedance amplifiers (TIAs).

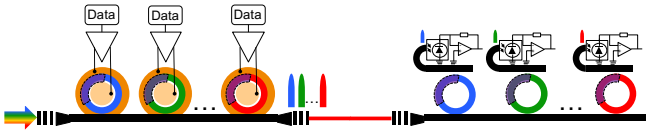

Figure 1. A block diagram of unidirectional ring-based SiP DWDM interconnect [21].

A. Grating Coupler

In the studied SiP link architecture, the light is coupled between the following pairs of photonic devices: the comb source and modulator, the modulator and fiber, and the fiber and demodulator. As we target high volume production, the photonic devices and circuits in this work are designed to be compatible with wafer-level characterization by using grating couplers (GCs) for optical IO, due to the easier probing access and lower mode mismatching compared to edge coupling. Recent improvements in single-polarization GC design achieved a minimum (peak) insertion loss (IL) as low as 1.35 dB [24], with a 1 dB bandwidth of 21 nm. The wavelength dependency of IL of a GC versus wavelength can initially be approximated by a second-order polynomial. This results in rapid growth of the GC loss beyond the 1 dB bandwidth, and as a result higher required comb optical power to compensate for the additional loss. In Ref. [25], a performance map of the coupling efficiency as function of 1 dB bandwidth of various C-band GC designs is provided. This map shows that the 1 dB bandwidth increases as the coupling efficiency decreases, a trend which has also been obtained in Ref. [26]. Unsurprisingly, as O-band and C-band GC designs are typically comparable in performance, a similar trade-off is observed in simulations of GCs designs in the O-band [27]. In this section, using a simple envelope-based performance model, we discuss the effects of this trade-off for two different classes of in-house GC designs, where each is optimized using adjoint method [28]. The first GC design is optimized for minimal peak IL by maximizing the GC coupling efficiency at its central wavelength, while the second GC design is optimized for double bandwidth at the expense of having a higher peak insertion loss by maximizing the mean GC coupling efficiency of two wavelengths near the edges of the targeted 1 dB bandwidth. The envelopes of the peak loss of each of the studied GC designs as function of the 1 dB bandwidth are shown in Fig. 2(a). The performance envelope of the first design is based on analysis of measurements, while the performance envelope of the second design is based on FDTD simulation. We estimated the peak loss envelopes as a second-order polynomial:

$$L_{\text{GC}}^{(\text{env})}[\text{dB}] = a \cdot B_{\text{GC}}^2 + b \cdot B_{\text{GC}} + c, \tag{1}$$

where B_{GC} is the 1 dB bandwidth with $IL_{1\,\text{dB}}$, and a, b, and c are the fitting coefficients. The minimum peak loss of the first design is $L_{\text{GC}_1} = 1.35\,\text{dB}$ with $B_{\text{GC}_1} = 21\,\text{nm}$, which is similar to the GC performance reported in Ref. [24]. On the other hand, the minimum peak loss of the second design is $L_{\text{GC}_2} = 1.85\,\text{dB}$ with $B_{\text{GC}_2} = 43\,\text{nm}$. These performances for O-band designs are in agreement with prior C-band GC design reported in Ref. [29]. In Fig. 2(b), the coupling efficiency performance curves of each of the GC designs at minimum peak loss, i.e., $L_{\text{GC}_1} = 1.35\,\text{dB}$ and $L_{\text{GC}_2} = 1.85\,\text{dB}$, are shown. It can be observed that the first design has lower loss over a wavelength range of $\widetilde{B}_{\text{GC}} \approx 17\,\text{nm}$ (derived from the crossing between the curves). However, beyond $\widetilde{B}_{\text{GC}}$ the loss of the first GC design increases rapidly compared to the second design. As a result, the total power penalty and losses of the link can be reduced further if the second GC design is used for links with DWDM bandwidth wider than $\widetilde{B}_{\text{GC}}$. Yet, the break-even point cannot be easily determined due to inconsistent trends of the total power penalties [30], [31]. Therefore, a detailed budget analysis is required to find the best GC configuration. More details on this analysis are provided in II-C.

B. Bus Waveguide

The small footprint of MRRs is beneficial when designing SiP modulators and demodulators [15]. In practice, the MRRs occupy a relatively small area in a ring-based transceiver design compared to other on-chip elements, e.g., PDs, and the pads required for the peripheral components, e.g., thermal

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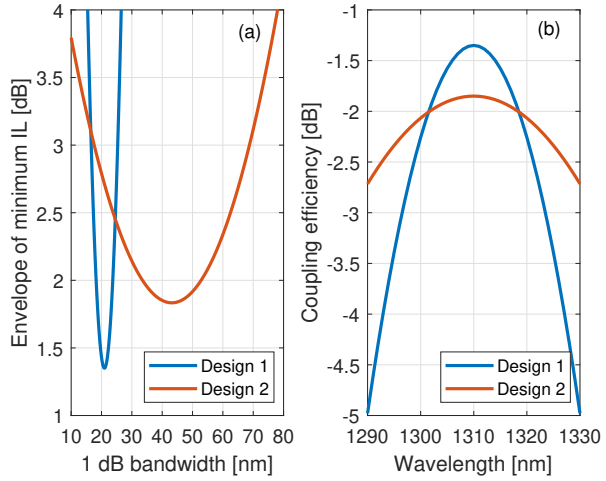

Figure 2. (a) Approximated envelopes of the minimum peak IL of the first and second grating coupler designs as function of 1 dB bandwidth. Each envelope follows a second-degree polynomial curve, where the coefficients for the first design are $a = 0.08669$, $b = -3.63544$, $c = 39.46529$, and the coefficients for the second design are $a = 0.00178$, $b = 0.1539$, $c = 5.1553$. (b) The coupling efficiency curves of the first and second grating coupler designs as function of wavelength. Each curve is calculated at minimum peak IL, i.e., $L_{\mathrm{GC}_1} = 1.35$ dB ($B_{\mathrm{GC}_1} = 21$ nm) and $L_{\mathrm{GC}_2} = 1.85$ dB ($B_{\mathrm{GC}_2} = 43$ nm). The first design has lower loss performance compare to the second design in a bandwidth of $\widetilde{B}_{\mathrm{GC}} \approx 17$ nm.

controller, drivers and TIAs. The pad size is dictated by the dimensions of the peripheral components and the assembly technology, e.g., wire-bonding. To minimize the RF mismatch loss, short RF high-speed transmission lines are required. Hence, the MRRs are organized as close as possible to the RF pads, and their spacing from one of each other is determined by the RF pads pitch. In our analysis, we are considering cascaded ring-based modulators and demodulators with 30-100 channels to achieve an aggregated data rate of 1 Tbps. This high channel count leads to a significant bus waveguide length, and as a result considerable insertion loss that cannot be ignored in the link budget analysis. Therefore, the bus length needs to be minimized. This can be attained by adopting advanced flip-chip assembly technology, which enables small pad area and pitch. In Ref. [21] a driver design with pad length, width and pitch of $40\,\mu$m has been discussed. This leads to a device length of $\sim 125\,\mu$m. Therefore, we assumed that the minimal distance between two adjacent MRRs centers is $125\,\mu$m. Recent advanced in flip-chip technology report on sub-$10\,\mu$m bump pad pitches [32], [33], which allows further reduction of the bus waveguide length. Moreover, the insertion loss of the bus waveguide can be reduced by improving its design. Here, we consider both uniform and hybrid etched bus designs. In the case of uniform etched design, which is illustrated in Fig. 3(a), the bus consists of a deep-etch waveguide (DEWG). Having a DEWG for the bus-waveguide is required, as the ring waveguide has a similar cross section, allowing for high confinement of the light in the ring waveguide cross-section. Consequently, a small minimal bend radii for the ring can be obtained, which results in a larger FSR, combined with a higher modulation efficiency. Instead, in the hybrid etched design, which is illustrated in Fig. 3(b), the bus along the directional coupler (DC) is DEWG, while the bus between adjacent bus-ring DCs is a medium-etch waveguide (MEWG). A MEWG is appealing for bus design due to its lower loss compared to DEWG. However, a hybrid etched bus design requires multiple medium-etch to deep-etch (ME/DE) tapers (compared to only two ME/DE tapers in a uniform bus design), where each is assumed to have a loss of $L_{\mathrm{ME/DE}} = 0.05\,\frac{\mathrm{dB}}{\mathrm{taper}}$. Note that in Ref. [34] even lower transition taper loss of $0.027\,$dB have been obtained. In addition, current designs of ME/DE tapers have noticeable reflections, which can become problematic when cascaded. A comparison analysis between the loss performance of the uniform and hybrid etched designs as a function of the number of channels is shown in Fig. 4(a), where the loss performance of the uniform and hybrid etched bus designs are calculated for the region A-B and A'-B', respectively, as illustrated in Fig. 3. In Ref. [35], a summary of the published waveguide loss performance of various silicon photonic platforms is provided. From this summary, the waveguide loss performance is in the range of 1-3.7 dB. Therefore, in our analysis, we assumed DEWG and MEWG losses of $L_{\mathrm{DE}} = 2\,\frac{\mathrm{dB}}{\mathrm{cm}}$ and $L_{\mathrm{ME}} = 1\,\frac{\mathrm{dB}}{\mathrm{cm}}$, respectively. The distance between two adjacent MRRs centers is $l_p = 125\,\mu$m, the DC and ME/TE taper lengths are $l_c = 30\,\mu$m and $l_t = 10\,\mu$m, respectively. The analysis shows that the uniform bus has significantly lower loss for any number of channels compared to hybrid bus. It is important to note that a narrow bus (330 nm) is considered for the bus of the DC. This might increase slightly the loss in both cases in these (short) bus waveguide sections. Also, a taper is required for the uniform etched design to minimize the mode mismatch between the narrow and standard bus waveguide widths. For a given taper footprint, additional reduction in taper loss is expected when advanced design techniques such as adjoint optimization are introduced [36]. Based on recent trends, we predict, though challenging, a ME/TE taper loss as low as $0.005\,\frac{\mathrm{dB}}{\mathrm{taper}}$ will eventually be achievable within a reasonably small footprint when using 139 nm immersion deep-UV (DUV) lithography, combined with advanced inverse design techniques [36], [34]. Given this taper loss, the analysis in Fig. 4(b) shows that the hybrid etched bus has slightly better loss performance. Decreasing the length of the DC can increase the difference in loss performance in favor of the hybrid etched bus design. Therefore, with future improvements in loss and reflection performance ME/DE tapers, a hybrid etched bus design can become a significant candidate to improve the link budget.

C. Power Budget Analysis

A crucial step in the design of cascaded ring-based SiP links is a detailed power budget analysis to determine the available link configurations. In the case of high performance computing (HPC) systems, a link configuration is feasible if the channel with the weakest received optical power at the input of the photodetector (PD) can be detected with a bit error rate (BER) better than 10^{-12}. In this work, we explored the available link configurations that can achieve an aggregated data rate

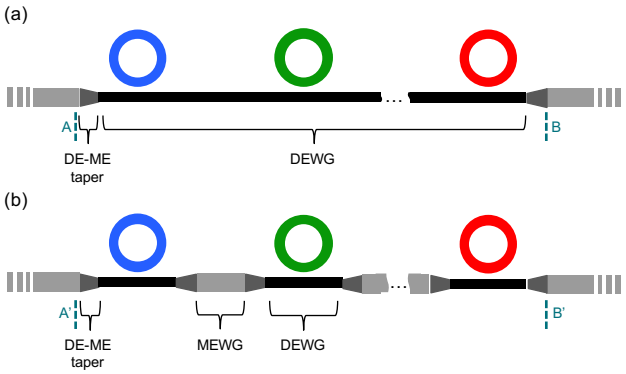

Figure 3. Bus waveguide design exploration. (a) Uniform etched bus design, where the bus of the DCs and between adjacent DCs is DEWG. (b) Hybrid etched bus design, where the bus of DCs is DEWG and the bus between adjacent DCs is MEWG.

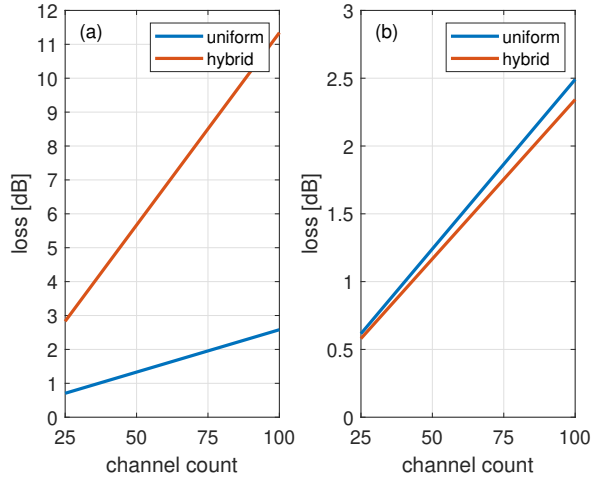

Figure 4. Bus waveguide loss analysis. The performance of uniform and hybrid etched bus designs are compared, where the waveguide parameters are $l_p = 125\,\mu$m, $l_c = 30\,\mu$m, $L_{\text{DE}} = 2\,\frac{\text{dB}}{\text{cm}}$, $L_{\text{ME}} = 1\,\frac{\text{dB}}{\text{cm}}$. The ME/DE taper has length of $l_t = 10\,\mu$m and loss of (a) $L_{\text{ME/DE}} = 0.05$ dB, and (b) $L_{\text{ME/DE}} = 0.005$ dB. The loss performance of the uniform and hybrid etched bus designs are calculated in the region A-B and A'-B' as illustrated in Fig. 3, respectively.

of 1 Tbps, where the design map consists of 30-100 channel count and channel spacing of $\Delta\lambda_{\text{comb}}[\text{nm}] = 0.2 + 0.1h; h \in \{0, 1, ...5\}$. This maps a design space of links with channel data rate of 10-33 Gbps and DWDM bandwidth of 6-30 nm, which are in the range of available and forecast technologies. At this point in time, the reported comb sources are limited in their ability to provide sufficient error-free lines (i.e., sufficient power to be detected by the PDs with BER $\leq 10^{-12}$) for fully integrated non-amplified 1 Tbps links [21]. Therefore, in our analysis we recovered the required optical power at the source-side to map the performance requirements of the comb sources. This is done by adding the total link power penalties and losses to the error-free PD sensitivity. The link budget includes the signal independent noise (SIN) and crosstalk power penalties, which are modeled using the power penalties expressions provided in Ref. [30], [31], and the coupling and bus waveguide losses, as described in Sec. II-A, II-B. We considered a narrow bus (330 nm) of the DC due to its weaker excitation of high-order modes and better coupling performance [13], which enables larger bus-ring gaps that are less sensitive to fabrication variations. The performance of the narrow bus of the DC are modeled using the behavioral model in [37]. At each point in the design map of channel count and spacing, we scanned independently the bus-ring gaps at the modulator- and demodulator-side and the extinction ratio (ER) of the modulation configuration, i.e., $g_{\text{TX}}[\text{nm}] = 110 + 10n$, $g_{\text{RX}}[\text{nm}] = 110 + 10k$, $\text{ER}[\text{dB}] = 10 + l$, where $n, k \in \{0, 1, ..., 9\}$ and $l \in \{0, 1, ..., 5\}$. The gap scanning on the demodulator-side is limited to filters with a 3dB-bandwidth higher than the channel data rate. At each link setting, we estimated the total power penalties and losses (PPL) to find the weakest channel: $\psi = \max\{\text{PPL}(R_b, \Delta\lambda_{\text{comb}}, g_{\text{TX}}, g_{\text{RX}}, \text{ER})\}$. Then, at a specific channel count and spacing, we searched for the best setting for which $\zeta(R_b, \Delta\lambda_{\text{comb}}) = \max\{\psi\}$. A map of ζ values within the FSR range (dashed curved) as function of the channel spacing and count is shown in Fig. 5 for MRR with $R = 3\,\mu$m. The inset is for MRR with $R = 5\,\mu$m. Both have $w_{\text{bus}} = 330$ nm, $w_{\text{ring}} = 450$ nm, $h_{\text{wg}} = 300$ nm, and $h_{\text{slab}} = 50$ nm. The dot-dashed curve stand for $\widetilde{B}_{\text{GC}}$ limit, where the second GC has a slower growth of the IL as a function of wavelength. The circle marker represents a link with the first GC design, while the rectangular marker represents a link with the second GC design that has better ζ performance than a link with the first GC design.

Given the PD sensitivity and link total power penalties and losses, the required optical power at the source-side can be estimated. Considering the sensitivity reported in Ref. [38], the required optical power of each of the comb lines $P^{\text{min}}_{\text{optical}}$ versus the comb bandwidth B_{comb} is shown in Fig. 6. The PD sensitivity, which is used to estimate PD_{sen}, is shown in the inset of Fig. 6. It is conservatively assumed that the PD sensitivity PD_{sen} below a channel data rate of 20 Gbps is $\text{PD}_{\text{sen}}(20\,\text{Gbps})$. The rhombus marker stands for a MRR with $R = 3\,\mu$m and the triangle marker stands for a MRR with $R = 5\,\mu$m. The number of channels is specified next to each of the markers. In [39] it is demonstrated that optical power higher than 6 dBm at the microring modulator, leads to high power penalty due to nonlinearity impairments. Experimental characterization of our microring modulators shows similar behavior. The analysis in Fig. 6 shows that only few configurations have a required optical power per comb tone less than 6 dBm, all with $B_{\text{comb}} \geq 12$ nm. Given $P^{\text{min}}_{\text{optical}}$, the total required optical power of the comb source $P^{\text{min,comb}}_{\text{optical}}$ versus the comb bandwidth is shown in Fig. 7. In Ref. [30] it is mentioned that the optical power in the silicon waveguide should be kept below $\sim$20 dBm to avoid nonlinearities in the bus waveguide. Yet, higher injected optical power might be possible if wider silicon waveguides, i.e., multi-mode waveguides, are used. From the analysis in Fig. 7, it can be observed that only few link designs require comb optical power less than 20 dBm where each of those configurations has $P^{\text{min}}_{\text{optical}} < 5$ dBm for the individual lines.

Mode-locked quantum dot (QD) comb lasers are considered as a promising type of DWDM sources for the next-

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generation 1 Tbps SiP links, due to their relative maturity, small footprint, and cost-effectiveness. The spacing between adjacent QD comb tones correspond to the cavity dimensions, which can be controlled to produce a precise intrinsic spacing of 25-100 GHz ($\sim$0.15-0.6 nm at 1310 nm)[1]. The tone count is regulated by their spacing and the total bandwidth of the comb. Current demonstrations of QD combs achieved a bandwidth of up to 10 nm [40], [41], [42]. Recently, the comb bandwidth has been improved to 13 nm by compensating for the group velocity dispersion (GVD). Yet, it is apparent that the bandwidth controlling mechanism of QD combs is not fully understood, as the gain material of this comb has a bandwidth of 50 nm. Thus, further study is needed to explain the comb physics in order to improve the control of its bandwidth. In addition, current Fabry Pérot QD laser can emit an optical power of 100 mW and higher [43]. Therefore, it is expected that a QD comb laser would be able to provide similar optical power. This optical power counts all the lines in the comb spectrum. Ideally, the power allocated equally between the tones within the comb bandwidth. However, in practice the power is distributed unequally between the tones across the spectrum, and as a result many of the lines do not have sufficient power for error-free performance. Therefore, the effective comb output power, which counts only useful tones, and in turn the effective wall plug efficiency (EWPE) are smaller than the measured optical power and wall plug efficiency (WPE) [21], [44]. Improved control over the number of tones above the required power threshold can be achieved if the comb bandwidth controlling mechanism is understood. In that case, a corresponding mirror can be designed as a reflective surface only for the comb bandwidth range, such that out of band tones are suppressed.

On-chip microresonator-based Kerr combs in the anomalous group velocity dispersion (GVD) regime have been widely studied [45], [46] and have recently been suggested as DWDM sources for integrated photonic links [19]. The spectrum of microresonator-based Kerr combs in the anomalous GVD regime follows a $\mathrm{sech}^2(\lambda)$ shape, which is undesirable for optical communications—for a DWDM comb source, spectral flatness (i.e., all tones have approximately the same optical power) is necessary to ensure that the maximal number of carriers are usable as information channels. Furthermore, pump-to-comb conversion efficiencies in anomalous GVD combs have been limited to < 5% and lack a clear path toward achieving greater efficiency. Recent demonstrations of microresonator-based comb formation in the normal GVD regime are promising, as they have exhibited much higher conversion efficiencies (up to 41% in Ref. [47]) while maintaining a relatively flat spectral shape. However, the pump-to-comb conversion efficiency does not account for the WPE of the pump laser, and therefore the actual energy efficiency of microresonator-based Kerr combs will be highly dependent on the characteristics of the pump laser.

[1]Based on the data sheet of Innolume comb laser LD-1310-COMB-8, https://www.innolume.com/_pdfs/Comb/LD-1310-COMB-8.pdf

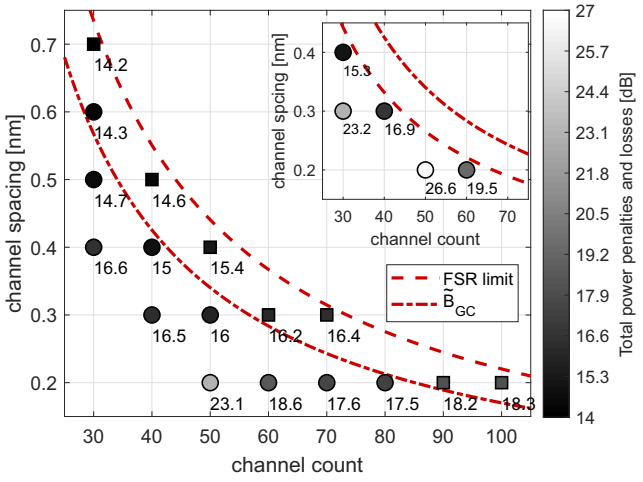

Figure 5. A map of the total power penalties and losses of various ring-based link configurations, each with different channel spacing and count. The marker color indicates the value of ζ, where the exact value is located next to each marker. The circle marker indicates available link configuration with the first grating coupler design. The rectangular marker indicates a link configuration with the second grating coupler design, which has lower ζ value compared to a link with the first grating coupler design. The dashed line is the FSR limit, and the dot-dashed line is the bandwidth of lower loss performance of the first grating coupler design compared to the second grating coupler design. The MRR parameters are $R = 3\,\mu$m (inset: $R = 5\,\mu$m), $w_{\text{bus}} = 330$ nm, $w_{\text{ring}} = 450$ nm, $h_{\text{wg}} = 300$ nm and $h_{\text{slab}} = 50$ nm.

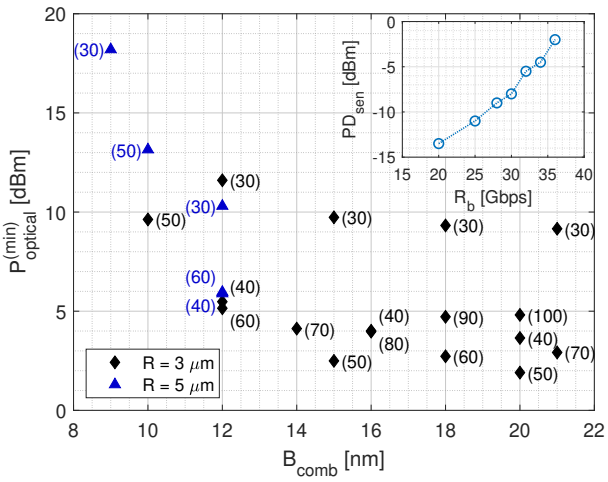

Figure 6. A design map of the minimum required optical comb line power as function of the comb bandwidth. $P_{\text{optical}}^{(\text{min})}$ is extracted from ζ (Fig. 5) and PD_{sen} reported in [38] (inset). It is conservatively assumed that the sensitivity at $R_b < 20$ Gbps is $PD_{\text{sen}}(20\text{ Gbps})$. The rhombus and triangle markers represent the $P_{\text{optical}}^{(\text{min})}$ of cascaded ring-based link with $R = 3\,\mu$m and $R = 5\,\mu$m, respectively. In both the MRR parameters are $w_{\text{bus}} = 330$ nm, $w_{\text{ring}} = 450$ nm, $h_{\text{wg}} = 300$ nm and $h_{\text{slab}} = 50$ nm. The value next to each link configuration marker specifies its channel count.

III. Energy Consumption Analysis

In this section, we estimate the energy consumption of the analyzed ring-based link as function of the channel data rate, R_b. The energy consumption analysis includes the comb source, drivers, MRRs thermal tuning at the transmitter- and receiver-side and the trans-impedance amplifiers (TIAs). The

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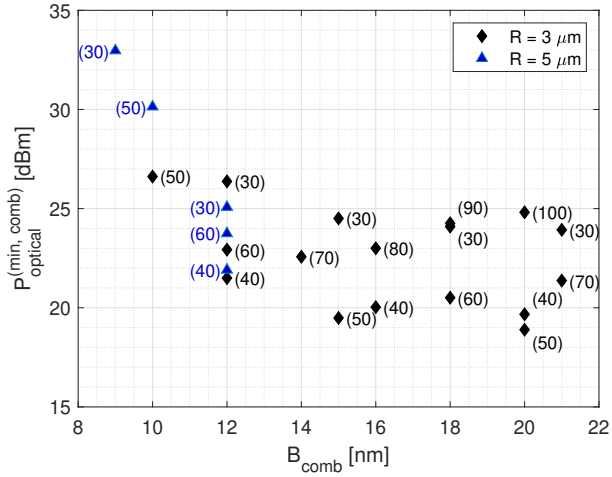

Figure 7. A map of the minimum required total optical comb power $P_{\text{optical}}^{(\text{min, comb})}$ as function of the comb bandwidth. The rhombus and triangle markers represent the $P_{\text{optical}}^{(\text{min, comb})}$ of cascaded ring-based link with $R = 3\,\mu$m and $R = 5\,\mu$m, respectively. In both the MRR parameters are $w_{\text{bus}} = 330\,$nm, $w_{\text{ring}} = 450\,$nm, $h_{\text{wg}} = 300\,$nm and $h_{\text{slab}} = 50\,$nm. The value next to each link configuration marker specifies its channel count.

required electrical power of the comb source is recovered from the performance map in Fig. 7 and the comb conversion efficiency. It is reported that QD comb laser reached to a wall plug efficiency (WPE) of up to 22% [20]. It is expected that a conversion efficiency of 40% and beyond can be achieved if improved QD gain media is used as in CW QD lasers [48]. In the case of microresonator-based Kerr combs in the normal dispersion (GVD), a pump-to-comb conversion efficiency of up to 41% is reported [47], where the pump source is an external continuous wave (CW) laser. However, the electrical-to-comb conversion efficiency is not provided, and we expect it be significantly smaller compared to the reported pump-to-comb conversion efficiency. It is important to note that the EWPE of comb laser, which counts only the optical power of tones above a given power budget $\mathcal{P}_b$ [44], is lower than the WPE. In Ref. [21] it is reported on maximum EWPE of 3.32% for $\mathcal{P}_b = 0\,$dBm. This low EWPE is due to a large number of tones with insufficient optical power above the required $\mathcal{P}_b$, while their total optical power is considerably larger such that the conversion efficiency decreases significantly. The unusable tones are located inside and outside the comb bandwidth. Therefore, the EWPE can be improved and get closer to the WPE if major number of tones within the comb bandwidth are usable, while the out of band tones have negligible total optical power. To increase the number of usable tones further improvement of the comb spectrum flatness and optical power per line is required. This can be achieved by better understanding of the bandwidth controlling mechanism of the comb laser as discussed in II-C. One may suggest using semiconductor optical amplifier (SOA) to amplify the line optical power, however this can lead to significant power penalty enhancement due to amplified relative intensity noise (RIN) of the laser. We expect that short-term improvements in the comb design can improve the EWPE to 10%. In the estimation of the minimum required comb electrical power, for each channel count (and in turn channel data rate) we identified the configuration of the MRR radius and channel spacing that has minimum comb optical power. The estimated comb electrical power for each channel data rate is shown by the rhombus marker in Fig. 8. To evaluate the total electrical power of the analyzed SiP ring-based link, we considered a 1-tap pre-emphasis driver designed for carrier-injection MRR [21], where each driver has power consumption of $P_{\text{D}} = (1 - \frac{\tau}{2})\frac{V_{\text{DD}}^2}{R_M + R_P}$ for equal transmission probability. The driver parameters are $\tau = 0.5 \cdot$ UI, $V_{\text{DD}} = 0.9\,$V (28 nm platform) and $R_M + R_P = 100\,\Omega$. It should be noted that two cascaded drivers are needed for channel data rates of ~ 20 Gbps and higher, which doubles the driver power consumption. Also, we considered a resistive microheater with thermal tuning efficiency of $20\,\frac{\text{mW}}{\text{FSR}}$ [49], which currently is the most efficient heater that is compatible with a standard CMOS platform [21]. The TIA power consumption is taken from [50] for 28 nm. In Fig. 8, the dotted, dot-dashed, and dashed curves stands for the power consumption of the driver, heater, and TIA. The circle marker in Fig. 8 represent the total energy consumption of the SiP ring-based link. The analysis indicates that a minimum energy consumption of $\sim 3\,\frac{\text{pJ}}{\text{bit}}$ can be achieved for $R_b = 25\,$Gbps. In order to obtain $E_b \leq 1\,\frac{\text{pJ}}{\text{bit}}$ as proposed by the energy efficiencies road map for the 2025 era [3], [4], [8], [10], further performance improvement of each of the link devices is required. For instance, better light coupling can reduce the required comb optical power and in turn the required electrical power. Improved tones utilization such that the EWPE is higher can also reduce the required comb electrical power. In addition, it is necessary to reduce the power consumption of the MRR heaters. This can be achieved by using advanced heaters designs, such as resistive microheater with substrate removal ($6.22\,\frac{\text{mW}}{\text{FSR}}$ [51]) or Ti heater with thermal isolation trenches and undercuts ($2.4\,\frac{\text{mW}}{\text{FSR}}$ [52]). for instance, in the case that the EWPE is 25% (improvement factor of 2.5) and a resistive microheater with substrate removal is used (improvement factor of 3.22), the energy consumption reduced to $1.37\,\frac{\text{pJ}}{\text{bit}}$ at 25 Gbps, which approaches the 2025 era proposed energy efficiencies.

IV. Conclusion

In this work, we analyzed a ring-based NRZ-OOK SiP link architecture for terabit-class communication. We provided an in-depth analysis of the trade-off between the peak IL and the 1 dB bandwidth of GCs. It is shown that increasing the GC bandwidth can potentially accommodate more spacious comb lines by reducing the attenuation on outer channels at the cost of a higher IL for the central channels. Additionally, we considered uniform and hybrid bus waveguide designs. We found that significant loss reduction of ME/TE tapers to meet the 1 Tbps requirements is needed. This can be achieved, for example, by applying novel adjoint design techniques in advanced DUV-immersion lithography nodes. When the loss performance of the ME/TE tapers are improved, the hybrid bus waveguide design becomes favorable for high channel count links due to the reduced propagation loss in the MEWG and for

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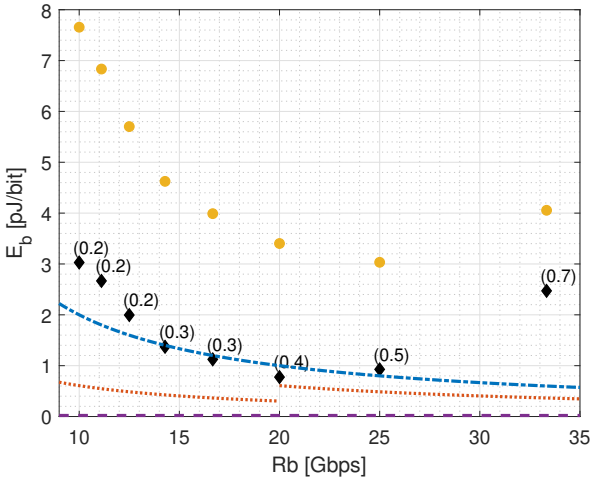

Figure 8. A map of the energy consumption E_b of the link devices for various data rates. The dotted curve, dotted-dashed curve, and dashed curve represent the E_b of the driver, ring heater at the TX (or RX) side, and the TIA. The rhombus marker represent the E_b of a cascaded ring-based link with $R = 3\,\mu$m. The value next to each comb configuration marker specifies its channel spacing in nanometers. The circle marker represent the total energy consumption including the comb, driver, TX and RX heaters, and TIA devices.

higher total optical powers due to the increased mode delocalization in the MEWG, resulting in lower peak field magnitudes and thus fewer nonlinear effects. We then comprehensively analyzed the power budget of various ring-based 1 Tbps link configurations, where each has a specific channel count and spacing. This allowed us to map the required optical power of the comb and each of its lines to provide a path to improve the performance of comb source for 1 Tbps SiP links under FSR and nonlinearity constraints. The maps show that only few configurations satisfy these constraints. In addition, based on the current progress of performance improvements, we expect QD comb lasers to be the first multi-wavelength source to achieve those requirements. Finally, the energy consumption of the ring-based SiP link is estimated based on current device power consumptions and near-future predicted electrical power performance of QD comb lasers. This analysis forecasts energy consumption as low as $3\,\frac{\text{pJ}}{\text{bit}}$. In the case of state of the art devices and improved comb EWPE, the energy consumption can be reduced to $1.37\,\frac{\text{pJ}}{\text{bit}}$, which is aligned with the 2025 era proposed energy efficiencies.

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