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Ultra-low power consumption silicon photonic link design analysis in the AIM PDK

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ABSTRACT

We demonstrate an optimized silicon photonic link architecture using components from the AIM PDK that achieves an ultra-low power consumption of 3.563 pJ/bit with an aggregate bandwidth of 400 Gb/s. At the transmitter, micro-disk modulators are cascaded along a bus waveguide to select and modulate wavelength-division multiplexed (WDM) channels. At the receiver, micro-ring resonator (MRR) filters are thermally tuned to match the corresponding disks to select from the multiplexed channels. This link architecture yields an ultra-small footprint compared to Mach-Zehnder designs, improving the system scalability and bandwidth density. Additionally, using micro-resonators to select and drop the desired wavelengths from a single bus waveguide allows for straightforward integration with a frequency comb source. The energy performance of the design is optimized through sweeping over three key parameters: (i) optical power per channel, (ii) channel count, and (iii) bitrate. These parameters are the dominant sources for the crosstalk and power penalty in the link design. We identify ideal points in the design space which minimize the energy per bit while staying below the desired bit error rate (BER) of 10^{-12} and maintaining a realistic aggregate bandwidth. Simulations in the Synopsys OptSim environment using the AIM PDK v2.5a models confirm the functionality of the system with a BER $< 10^{-12}$, acceptable for both high performance computing (HPC) and data center (DC) applications. Furthermore, optimizing the link energy consumption in the AIM PDK provides a clear path towards low-cost and high-yield fabrication suitable for application in HPC and DC systems.

Keywords: Interconnects, Transceivers, AIM

1. INTRODUCTION

The rapid rise of data-intensive applications such as machine learning and artificial intelligence has placed exponentially growing demands on the bandwidth of interconnects in high performance computing and data center systems.[1] Silicon photonics poses an attractive solution to this bandwidth requirement by providing a high bandwidth and energy-efficient platform for optical interconnects.[2] Furthermore, the silicon photonics platform is low-cost as it takes advantage of the mature and widespread CMOS infrastructure used for microelectronics fabrication. However, for silicon photonics to mature into a commercially viable solution for HPC and DC interconnects, it requires a platform that enables the full product lifecycle from research and development through volume manufacturing with the ability to quickly prototype and validate designs.

Process design kits (PDKs) provide validated device models specific to the foundry, enabling photonic integrated circuit (PIC) designers to focus on system-level integration without the need to also design custom components.[3] Furthermore, multi-project wafer (MPW) runs lower the cost barrier associated with fabrication by allowing customers to "share" the wafer and thus quickly prototype PICs without the large investment of purchasing a dedicated one-to-one run. The combination of PDK libraries and MPW runs provided by foundries allows for the rapid design and fabrication of complex PICs with a high likelihood of the desired functionality on the first try.

Here, we explore the design space for silicon photonic links based on a cascaded MRR architecture using elements available in the American Institute for Manufacturing for Integrated Photonics (AIM) PDK to identify

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optimized configurations that yield the highest energy efficiency. Using validated compact models provided in the AIM PDK v2.5a, we perform S-parameter simulations in the Synopsys OptSim environment to scan over possible valid link configurations and calculate the total power consumption of each. We identify ideal points in the design space that minimize the energy per bit while also maintaining a realistic aggregate line rate for use in ultra-low energy, high-bandwidth HPC and DC optical interconnects.

2. LINK ARCHITECTURE

2.1 Overview

The transmitter is composed of micro-disk modulators (MDMs) cascaded along a bus waveguide, with each modulator corresponding to an individual WDM channel.[4,5] The wavelength-selective nature of resonant micro-disk cavities is exploited to modulate the desired wavelength channel, removing the need to demux the channels for modulation. Modulation is achieved by injecting carriers into the micro-disk, tuning its effective index (and thus the resonant wavelength) through the plasma-dispersion effect.[6] The modulated channels are then coupled out of the transmitter PIC into single-mode fiber and sent to the receiver PIC. The light is then coupled into the receiver PIC, which is similarly composed of MRR drop filters cascaded along a bus waveguide. Again, the MRR filters are tuned to match the desired channel wavelength and selectively drop each channel from the bus, which are then incident on respective photodiodes (PDs) to convert the optical signal back into the electrical domain.

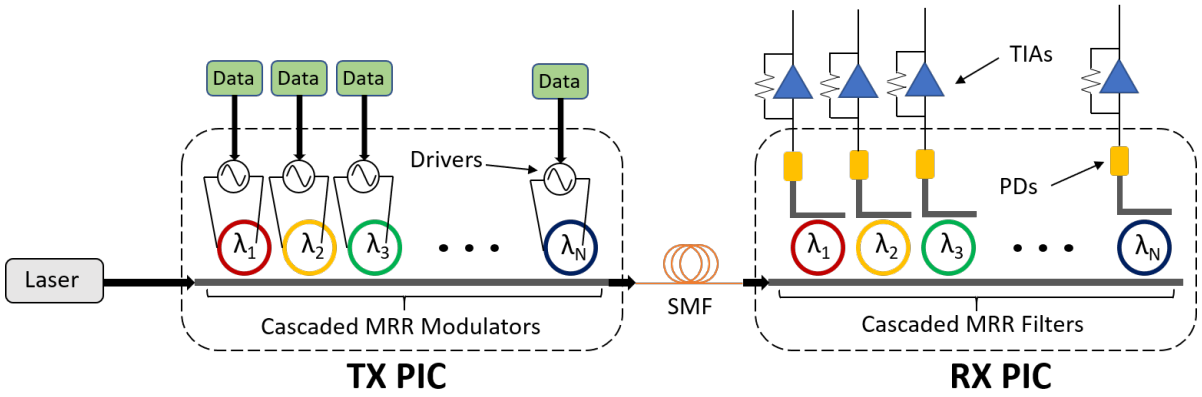

Figure 1: Schematic of the point-to-point unidirectional link architecture for N channels.

Using MDMs and MRRs to perform the modulation and filtering yields a small footprint and highly scalable architecture. Furthermore, using cascaded rings to select wavelength channels from the bus waveguide is desirable when using a frequency comb source as it removes the need to demux the large number of generated wavelength channels before modulation.[7,8] Recent advances in frequency comb generation in silicon nitride (Si_3N_4) MRRs opens the possibility of monolithically integrating the source on the transmitter PIC, reducing the footprint and packaging complexity while also removing the difficulties associated with coupling alignment.[9]

2.2 Design Considerations

To construct an energy efficient, high-bandwidth link using this architecture, it is necessary to consider both the properties of the individual devices (MDMs, MRRs, PDs, etc.) as well as the system parameters (channel count, channel spacing, bitrate, and optical power). At the device level, the free spectral range (FSR) of the MDMs and MRRs poses a constraint since if the wavelength band exceeds one FSR, significant channel overlap is introduced.[10] The FSR of the MDMs and filters in the AIM PDK is 25.6 nm, so the difference between the largest and smallest channel wavelengths cannot exceed this number. Additionally, the quality factor (Q) of the MRRs restricts the channel spacing, as the 3dB bandwidth for low Q MRRs is large and results in overlap in the resonances for small channel spacings.

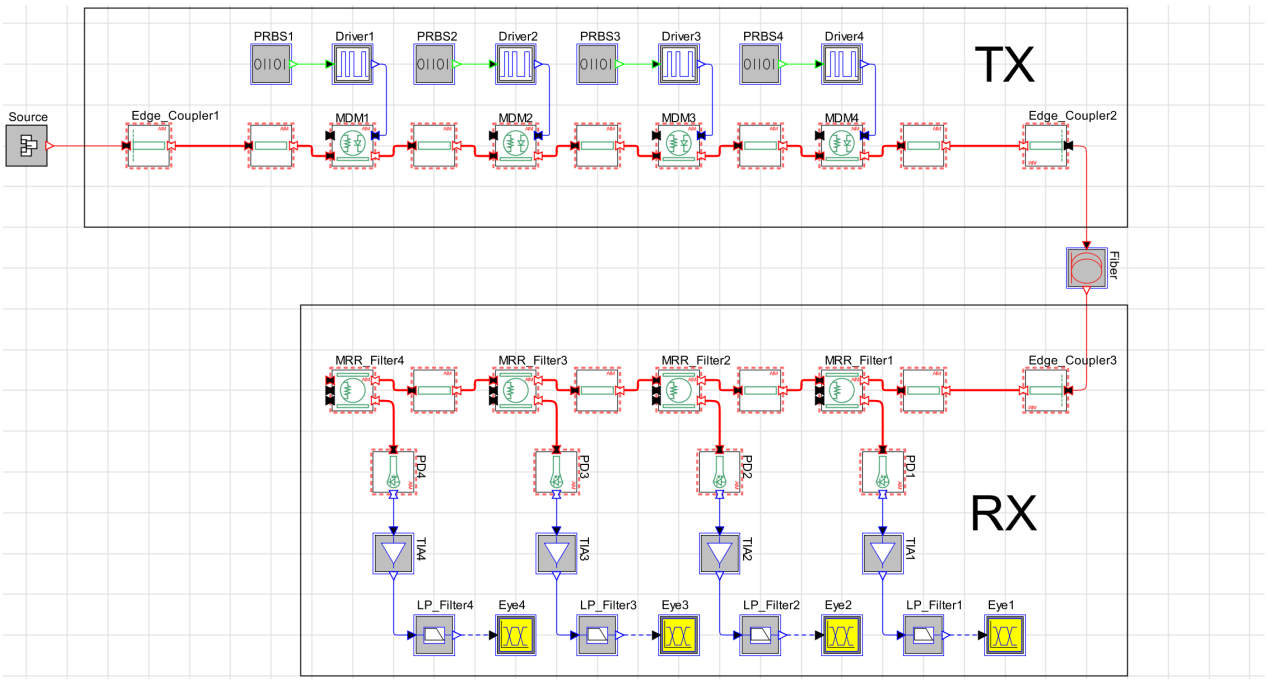

Figure 2: Schematic view in OptSim for a 4 channel link architecture.

At the system level, there is a tradeoff between the maximum modulation rate and the channel spacing, as the 3dB bandwidth of the MRRs must be large enough to drop the modulated signal without filtering out the information contained in the sidebands which increases the channel crosstalk as channel spacing is reduced. Additionally, increasing the bitrate requires increased optical power to overcome the frequency-dependent responsivity of the PDs.

3. POWER CONSUMPTION MODELS

3.1 Laser Source

The required optical power from the source for each channel is determined by the power penalty of the link, the receiver sensitivity, and the desired margin, where the margin is added to account for fluctuations in the other values so the optical power remains above the threshold and the signal integrity is not compromised.[11] We assume a wall-plug efficiency (WPE) of 10% for each laser source, yielding an electrical power consumption for each channel of ten times the optical output power. Additionally, we limit the maximum optical output power in our simulations to 5 mW per channel due to the optical nonlinearities of MRRs.[12]

3.2 Modulation

We consider a non-return-to-zero on-off keying (NRZ-OOK) modulation format with a 1 V_{PP} driving voltage for each MDM.[13] For the energy consumption of the drivers, we assume a linear first order empirical model given by[12,14]

$$E \approx a \times \text{bitrate} + b \tag{1}$$

where E is the energy consumption per bit [J/bit] and the constants a and b are calculated as

$$\begin{aligned} a &= 1.4 \times 10^{-23} \times \left(\frac{V_{PP}}{2V_{DD}}\right)^2 \times \left(\frac{C_{mod}}{C_{ref}}\right) \\ b &= 8.4 \times 10^{-14} + \frac{1}{4}\left(C_{mod}V_{PP}^2 - C_{ref}(2V_{DD}^2)\right) \end{aligned} \tag{2}$$

where V_{DD} is the supply voltage, C_{mod} is the equivalent capacitive load of the MDM, and C_{ref} is the capacitance of the reference capacitor.

3.3 Thermal Tuning

The thermal efficiency for the MDM heaters is 0.54 nm/mW and 1 nm/mW for the MRR filter heaters. To minimize the power dissipation from thermally tuning each resonance, the AIM PDK provides four modulators and four filters with identical performance characteristics and center wavelengths of 1550 nm, 1556.4 nm, 1562.8 nm, and 1569.2 nm. When scaling to channel counts above four, the additional channels are tuned to be between these fixed wavelengths such that there are always four channels that expend no thermal tuning energy. In a real system, the fixed channels will not be exactly at the specified wavelengths due to fabrication variations, but we assume the thermal tuning to correct these variations is negligible compared to the thermal tuning required to bias new channels between the fixed wavelengths.

3.4 Receiver

The AIM PDK PD has a responsivity of 1 A/W and 43 GHz 3dB bandwidth for a -1 V bias. In addition to the PD, the receiver also requires a transimpedance amplifier (TIA) to convert the photocurrent from the PD into a voltage signal. To calculate the TIA power consumption, we use a database of optimized TIA topologies in 65 nm CMOS in lieu of an analytical model.[15] For a given bitrate, we select the most energy efficient TIA design from the database.

4. LINK SIMULATION AND ENERGY ANALYSIS

The channel count and channel spacing are tightly coupled for the described architecture; the four default MRRs and MDMs in the AIM PDK consume no thermal power, so these wavelengths (1550 nm, 1556.4 nm, 1562.8 nm, and 1569.2 nm) are used in all possible designs. Since all new channels are tuned between these wavelengths, in order to maintain uniform channel spacing, all valid channel counts must be multiples of four. We performed simulations for all valid channel counts from 4 (6.4 nm spacing) to 32 (0.8 nm spacing) channels, sweeping the data rate per channel from 10 GHz to 25 GHz and the optical input power per channel from 1 mW to 5 mW. For each configuration of the sweeps, we used the simulated eye diagrams and Monte Carlo BER estimation to ensure that the BER remained above 10^{-12} for all channels (Figure 3). The receiver sensitivity was calibrated to yield a BER of 10^{-12} for -17 dBm incident optical power for a 10 GHz signal.

Table 1: Optimal energy configurations for different channel counts.

Channel Count	Spacing (nm)	Energy per bit (pJ/b)	Data Rate (Gb/s)	Aggregate BW (Gb/s)
4	6.4	1.056	12.5	50
8	3.2	1.426	15	120
12	2.133	2.135	15	180
16	1.6	2.554	17.5	280
20	1.28	2.321	15	300
24	1.067	2.459	12.5	300
28	0.914	3.712	12.5	350
32	0.8	3.563	12.5	400

For all configurations that satisfy the BER requirement, we then calculated the energy per bit using the models presented in the previous section. Table 1 shows the resulting optimal points of the design space for each channel count that minimizes the energy per bit. It is clear that the 4 channel link yields the best energy efficiency, but at the cost of aggregate bandwidth—the optimal 32 channel configuration yields an aggregate bandwidth of 400 Gb/s with an additional 2.5 pJ/b compared to the 4 channel case.

Figure 3 shows the difference in the design space for the two boundary cases (4 channels and 32 channels) by first finding the bitrate for each that leads to a BER $> 10^{-12}$ (subfigures (a) and (b), respectively) and then limiting the regions of the energy per bit design space to exclude the points where the BER requirement is violated (subfigures (c) and (d), respectively).

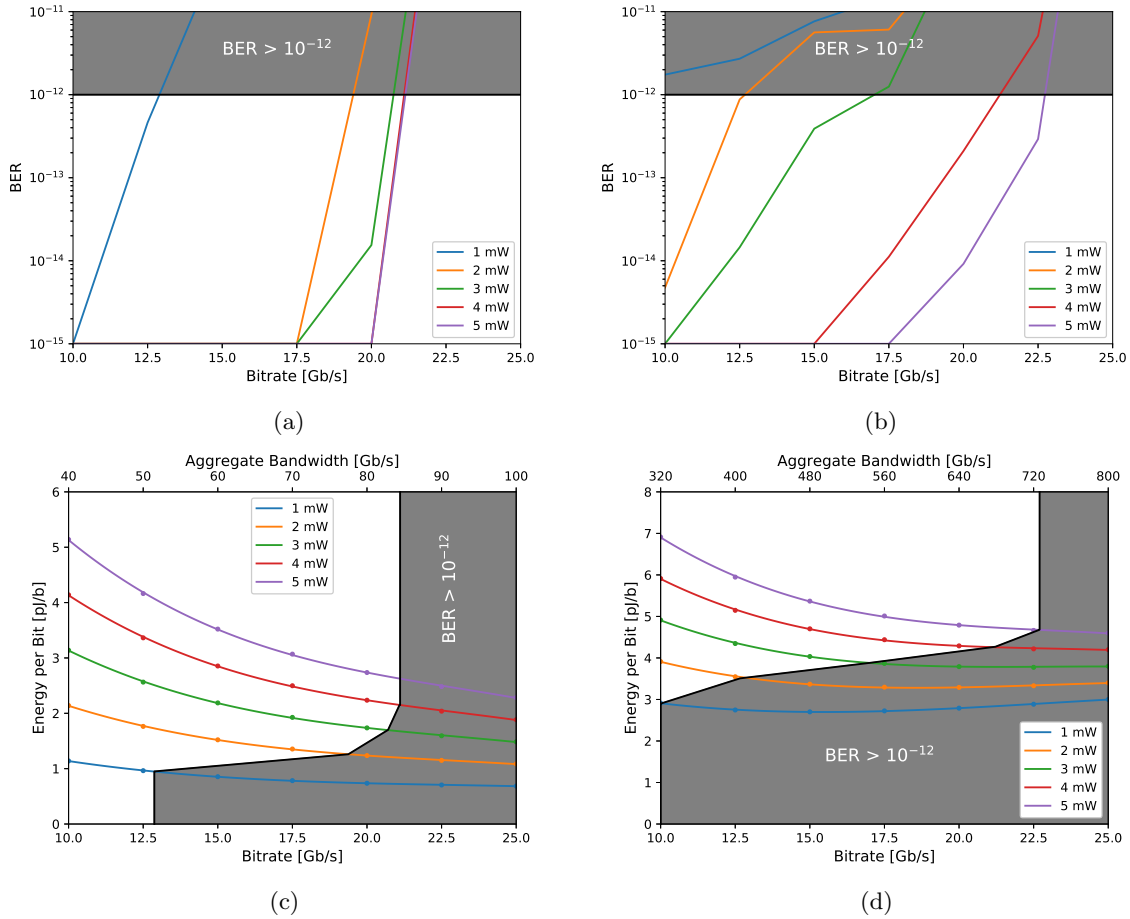

Figure 3: Identification of error-free link configurations for (a) 4 channels and (b) 32 channels, and comparison of the energy per bit versus bitrate for the error-free configurations for (c) 4 channels and (d) 32 channels. The gray regions indicate points in the design space that violate the BER requirement.

5. CONCLUSION

We explored the design space of ultra-low energy silicon photonic links based on a cascaded MRR architecture using AIM PDK components and identified key points that yield optimal energy efficiency while maintaining error-free operation. While restricting the design space to a PDK library allows for straightforward optimization at the system level, it does not take full advantage of recent advances in devices. For example, Intel has recently demonstrated a 128 Gb/s micro-ring modulator (MRM) with a 50 GHz electro-optic bandwidth and 0.52 V·cm phase efficiency.[16] Therefore, to achieve truly state-of-the-art system performance, it is essential for PDK libraries to keep pace with device advances. The optimization process outlined in this work can be easily adapted to accommodate these advances provided the validated compact models for the devices.

This analysis using the most recent AIM PDK models (v2.5a) characterized key dependencies of the link performance on the bitrate, channel spacing, and optical power. Simulation results show that error-free operation can be expected for optimal link configurations with up to 400 Gb/s aggregate bandwidth and 3.563 pJ/bit energy consumption.

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