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### Design Considerations for Multi-Chip Module Silicon Photonic Transceivers

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ABSTRACT

High bandwidth density silicon photonic interconnects offer the potential to address the massive increase in bandwidth demands for data center traffic and high performance computing. One of the major challenges in realizing silicon photonics transceivers is the integration and packing of photonic ICs (PIC) with electronic ICs (EIC). This paper presents our version one, 2.5D integrated multi-chip module (MCM) transceiver for 4 channel wavelength division multiplexing (WDM) operation, targeting 10 Gbps per channel. We identify five key areas critical to successful integration of MCM transceivers, which we have used in developing our version two MCM transceiver: integration architecture, equivalent circuit model development, PIC to EIC interface modelling, MCM I/O design, and design for assembly.

Keywords: Silicon Photonics, Multi-Chip Module, Interposer, 2.5D Integration, Optical Interconnects, Wavelength Division Multiplexing

#### **1. INTRODUCTION**

Data center and high-performance computing interconnects are faced with ever increasing bandwidth demands as the rise of compute intensive artificial intelligence and machine learning is coupled with exponentially growing internet traffic<sup>1</sup>. Further, required I/O bandwidths are outpacing the growth of I/O pins per package<sup>2</sup>. While interconnect bandwidths can be increased by increasing the electrical data rates, higher rates that push the channel limits can require significant equalization circuitry, which increases the energy consumption of the transceiver. However, there are effective maximum data rates at which the energy required to implement the equalization circuitry to achieve the desired data rate makes the design unfeasible<sup>3</sup>. Silicon photonics offers a potential solution to the exponentially increasing bandwidth due to high bandwidth links, natural channel parallelization through wavelength division multiplexing (WDM), energy efficiency, marginal signal attenuation, and ability to leverage the mature CMOS infrastructure<sup>4</sup>.

While silicon photonics can help address the growing data center and high-performance computing demands, integrating the photonics with both the compute circuitry and the driving circuitry remains a crucial step in developing silicon photonic transceivers. Ineffective integration with the electronic circuitry can negate any potential benefit from the silicon photonics. In this paper, we outline five key design areas that need to be addressed when developing silicon photonic transceivers: integration architecture, equivalent circuit model development for the photonic components, model for the PIC to EIC interface, MCM I/O design, and design for assembly. We then provide an overview of our 2.5D integrated, WDM multi-chip module (MCM) transceiver designs, and highlight the performance of our first transceiver version.

#### 2. MCM TRANSCEIVER DESIGN

Our transceiver architecture is based around microdisk photonic elements coupled to a bus waveguide for WDM operation. On the transmit side, microdisk modulators with integrated heaters are coupled to a bus waveguide with taps placed after the modulators with monitor photodiodes to provide for thermal calibration input signals. On the receive side, demultiplexing microdisks coupled to the bus waveguide have drop ports to high speed photodiodes. At the end of

Metro and Data Center Optical Networks and Short-Reach Links III, edited by Atul K. Srivastava, Madeleine Glick, Youichi Akasaka, Proc. of SPIE Vol. 11308, 113080I · © 2020 SPIE CCC code: 0277-786X/20/\$21 · doi: 10.1117/12.2544008 the bus waveguide, a monitor photodiode is used to provide a thermal calibration input signal. The photonic integrated circuits were fabricated though AIM Photonics using the AIM process design kit (PDK). This architecture was pursued because it presents a platform for high areal bandwidth density, high total throughput, and high energy efficiency. The high areal bandwidth is achieved by fabricating microdisks with small area—diameters below 5 µm have been demonstrated<sup>5,6</sup>. High total throughput is achieved by a combination of the small area and the resonance behavior of microdisks coupled to the bus waveguide providing a natural platform for dense wavelength division multiplexing (DWDM). The architecture is energy efficient due to the microdisks low junction capacitance and low drive voltages compared to Mach-Zehnder modulators<sup>7</sup>. Additionally, the highly parallel DWDM allows for the individual channels to run at lower data rates—avoiding the need for power hungry equalization and signal processing circuits, and potentially avoiding the need for SERDES. For these reasons, we targeted 10 Gbps per channel.

Two prototype versions for this transceiver architecture were fabricated. Both prototypes featured 2.5D integration with a silicon interposer: both PIC and EIC bare dies were flipped onto an interposer which was used to provide the connectivity between them and interface to a PCB for I/O and for control signals. Version one featured four channels on the both the transmitter and receiver and utilized commercial bare die TIAs on the receive side to interface to the PIC's photodiodes. For this design, the interposer I/O was not impedance controlled. Version two features six channels, custom TX and RX EICs, and impedance controlled impedance traces. On the TX side, the EIC interfaces to the microdisk modulators and performs PRBS generation, serialization, and signal amplification. On the RX side, the EIC interfaces to the PIC's photodiodes and features a TIA, signal amplification, and deserialization.

The packaged device for the version one prototype can be seen in figure 1 a). The eye diagrams for both the transmit microdisk modulators and receive TIA output can be seen in figure 1 b) and 1 c). The data rate for both the transmitter and receiver were 7 Gbps. This data rate was limited, likely due to the prototype's bandwidth being limited due to interposer parasitics and lack of impedance control. The version two prototype is currently being packaged. In the following section, we will outline the design steps taken in developing the version two prototype, with an emphasis on improving the bandwidth of the transceiver.



Figure 1. a) The packaged version 1 MCM transceiver prototype utilizing commercial TIAs. b) The eye diagram from the receiver at 7 Gbps. c) The eye diagram from the transmitter at 7 Gbps.

#### 3. CRITICAL AREAS OF MCM TRANSCEIVER DESIGN

#### 3.1 Integration Approach

The integration architecture for an MCM transceiver directly impacts the transceiver's areal bandwidth, edge bandwidth, and packaging parasitics. These metrics constrain the transceiver's total bandwidth, energy consumption, and performance. While silicon photonics can address the bandwidth demands in data centers and high-performance

computers, the benefits can be negated if the MCM transceiver is not integrated appropriately. The main integration approaches for silicon photonic MCM transceivers are monolithic, 2D, 3D, and 2.5D. Monolithic integration is defined as when both the driving electronic circuits and the photonic components are fabricated within the same process, as shown in figure 2 a). This approach offers the minimum parasitics, as the photonics and electronics can be tightly integrated with only microns of separation. Additionally, the packaging for monolithic integration is the most straightforward, as separate EICs and PICs don't need to be integrated by an additional fabrication process. The main drawback of monolithic integration is the difficulty of developing a process that is simultaneously optimized for photonic performance and electronic performance. The monolithic integrations are built on older CMOS nodes—the most cutting edge is a 32 nm node demonstration that is still under development<sup>8</sup>. The alternative to monolithic integration is hybrid integration, where the EIC is fabricated in an electronic-only process and the PIC is fabricated in a photonic-only process. Photonic performance in monolithic processes lags compared to photonic-only process can be prohibitively expensive when compared to separate processes with hybrid integration.



Figure 2. The four integration architectures outlined. a) Monolithic integration with the EIC and PIC fabricated in the same die. b) 2D integration, where the PIC and EIC are placed side-by-side and connected via wirebonds. c) 3D integration, where the EIC is flipped on top of the PIC and connected with micro solder bumps or copper pillars. d) 2.5D integration, where the EIC and PIC are both flipped on top of an interposer, which provides the connectivity between them.

With 2D integration, the PIC and EIC are situated adjacent to each other and connected by wirebonds, as shown in figure 2 b). This approach is the most straightforward hybrid integration, but introduces comparatively high parasitic inductance, as wirebonds typically have 0.5 - 1.0 nH/mm<sup>9</sup>. Additionally, 2D places a limit on I/O, as connections between the PIC and EIC can only be made on the shared edge, which can limit total bandwidth. 3D integration can be used to increase the I/O between the PIC and EIC, as the I/O connections are no longer limited to a single edge, as shown in figure 2 c). The I/O connection can be made with microsolder bumps or copper pillars, with pitches down to 50 µm or below<sup>10-12</sup>. In addition to increasing I/O, parasitics are reduced compared to 2D integration, as the bumps have parasitic capacitance below 30 fF<sup>10,11</sup>. One of the drawbacks of 3D integration is the poor thermal isolation between the PIC and EIC. PICs have been observed to vary by 20 °C in the presence of a driving EIC<sup>13</sup>, which can introduce operational challenges to thermally sensitive microdisk resonant photonics. Additionally, interfacing the driving electronic integrated circuits of a 3D integrated MCM to compute integrated circuits introduces similar drawbacks as 2D integration. Wirebonds from the MCM will introduce inductive parasitics and limit I/O. A final hybrid approach is 2.5D integration, where both the PIC and EIC are flipped on top of an interposer, as shown in figure 2 d). An interposer is a thin substrate that serves as electrical redistribution, and can be constructed from silicon, organics, or glass. In the case of a silicon interposer, through silicon vias (TSVs) can be used to connect to the back side of the interposer to interface to a PCB or another substrate. The benefits of 2.5D integration are that it enables high I/O counts with microsolder bumps or copper pillars at the same pitches as 3D integration, while also providing a platform for further scalability by allowing compute integrated circuits to be flipped on the same interposer or interfaced through the connections on the backside of the interposer. A drawback of the 2.5D integration is that the parasitics at the interface between the PIC and EIC will be larger, as signals must pass through a pair of bumps and the trace on the interposer.

#### 3.2 Photonic Equivalent Circuit Model

Developing integrated MCM transceivers requires close co-development of the photonic components with the electronic driving circuits. While commercial electronic drivers can be purchased, to develop energy efficient transceivers with the highest performance, the driving circuitry needs to be developed to match the specific photonic components. In order to design around the specific photonic components (modulators and photodiodes), compact equivalent circuit models for these components need to be developed. Equivalent circuit models can vary widely in complexity; it is best to make the model as simple as possible, while still capturing the physical properties of the components, to avoid creating a model susceptible to overfitting<sup>14</sup>. Models can be as simple as a resistor and a capacitor in series to model a silicon photonic depletion phase shifter<sup>15</sup>. The capacitor represents the PN junction capacitance and the resistor represents the series resistance of the slightly doped P/N silicon and the contact resistance to the silicon. Such a model doesn't include parasitics, pad models, or trace models, but serves as a first order model that is adequate for some applications. More complex models can be developed for transmission line equivalent circuits for travelling wave carrier depletion phase shifters in Mach-Zehnder modulators. These models can include tens of individual circuit components in the equivalent model<sup>16,17</sup>, and are required to be distributed models rather than lumped models to account for the changing phase across the photonic component. Additional silicon photonic equivalent circuit models have been developed and fit for electroabsorption modulators<sup>18</sup>, microring carrier injection modulators<sup>19</sup>, microring carrier depletion modulators<sup>20,21</sup>, and Germanium photodetectors<sup>18,20,22</sup>.



Figure 3. a) The equivalent model used for the modulator, showing the probe, pad, trace, and modulator junction components. b) The Smith chart showing the measured and model data for the S11 measurement. c) The S11 magnitude measurement showing the measured and model data.

In developing our model, we followed the base model outlined by G. Li *et al.*<sup>21</sup>. The base model, along with additional circuit components added to reflect our layout and measurement setup, can be seen in figure 3 a). The C<sub>J</sub> and R<sub>S</sub> represent the modulator's junction capacitance and the series resistance from the doped silicon and contacts to the silicon, respectively. The C<sub>P</sub> represents parasitic capacitances. The C<sub>Pad</sub> and R<sub>Pad</sub> represent the capacitance from the pads to the silicon substrate and the resistance within the substrate, respectively. Inductance components were added between the pad portion and the modulator portion. Additionally, a RF probe was used to measure the device—parasitic inductance, resistance, and capacitance were added to the model, as well as the transmission line length component to account for the phase dependence across the frequencies of interest.

The modulator was probed with a GSG FormFactor RF probe. A precision network analyzer (PNA) was used to measure the S11 of the modulator. Biasing the modulator to the operating 0.5 V reverse bias was achieved with a bias-T in between the PNA and the RF probe. The measurement setup was calibrated with a calibration kit up to the probe input. The S11 measurement was recorded from DC to 40 GHz for several DC bias voltages. The S11 data was used to fit the model, shown in figures 3 b) and 3 c), using ADS. Key values extracted from this process are 93 fF for C<sub>J</sub>, 55 fF for C<sub>P</sub>, and 133  $\Omega$  for R<sub>s</sub>. For future work, we intend to model the photodiode used in the MCM transceiver, utilize a on chip calibration substrate to allow for a simpler model, and use a lightwave network analyzer so S21 parameters can also be measured.

#### 3.3 PIC to EIC Interface

Similar to developing the equivalent circuit models for the active photonic elements, it is necessary to model the parasitics of the interface between the driving circuits in the EIC and the active photonic elements to achieve high performance interconnects. For 2D integration, the wirebond connecting the PIC and the EIC can essentially be modelled by an inductor, with the inductance per mm ranging between 0.5 and 1.0 nH<sup>9</sup>. Some models can include resistive elements and capacitive elements for the pads<sup>23</sup>, but should not be included if the pads are already incorporated into the photonic equivalent circuit. The parasitics for micro solder bumps and copper pillars tends to be quite small—negligible inductance, less than 1  $\Omega$  of resistance, and less than 30 fF of capacitance<sup>24,25</sup>. While small, the bump's parasitic capacitance is still within the same order of magnitude as the equivalent model's junction capacitance and parasitic capacitance for both the photodiode and disk modulator. This parasitic capacitance is especially important on the receiver portion of the transceiver, as the total capacitance—photodiode junction capacitance, photodiode parasitic capacitance, and bump parasitic capacitance—dictate the dominant pole of the transimpedance amplifier (TIA), which impacts the TIA's bandwidth<sup>26</sup>.

Moving to 2.5D integration increases the parasitics for the PIC to EIC interface. The interconnect will have two bumps rather than one, and the trace on the interposer also introduces additional parasitics. To determine the parasitics for our 2.5D MCM transceiver with custom EICs, the S parameters for the interposer trace were simulated using EMX up to 40 GHz. Initially, we intended to fit the S parameters to a simple pi-model, as shown in figure 4 a). Initial results produced a pi-models with several  $\Omega$  for the resistor, less than one nH for the inductor, and tens of fF for each capacitor. However, the pi-model did not fit the simulated S parameters very well. There was also concern that the interposer's trace has parasitic capacitance and inductance distributed across the trace, rather than the consolidated representation of the pi-model. To better reflect the physical model of the interposer trace, the S parameters were fit to a 30-pole rational polynomial HSpice model using ADS. The resulting model featured over 1000 components to accurately model the interposer trace. The simulation S parameters for one interposer trace can be seen in figure 4 b). The pi model's S parameters can be seen in 4 c) and the multi-pole HSpice model's S parameters can be seen in 4 d). The multi-pole HSpice model accurately models the simulated S parameters, while the Pi model begins to diverge after 15 GHz.



Figure 4. a) The S parameter, pi model, and multi pole HSpice model for a data trace on the interposer between the PIC and EIC. The pi-model's parameters were fit with Matlab, and the multi-pole HSpice model was fit in ADS. b) The simulated S parameters for the interposer trace. c) The S parameters from the pi-model. d) The S parameters for the multi-pole HSpice model.

#### 3.4 MCM I/O

Designing a silicon photonic MCM transceiver requires careful consideration with regards to how the I/O data interfaces electrically to the transceiver. Improper design of the I/O can limit the transceiver's performance, potentially negating innovations in the PIC and EIC. Improper I/O can introduce parasitics and impedance mismatches that limit system performance. The I/O choices will depend on the MCM integration approach.

For 2D or 3D integration, wirebonding is the most common approach to interface to the MCM transceiver. The main drawback of wirebonding is the parasitic inductance from the bond: it is typically between 0.5 and 1.0 nH/mm<sup>9</sup>. Additionally, wirebonds are typically restricted to the edges of the chips. If the design requires a large number of connections, the larger required fanout will increase the parasitics and enlarge the impact of impedance mismatch. Wirebonds connections can be made as dense as  $25 \,\mu\text{m}$  pitches<sup>27</sup>, but the tradeoff is that denser pitches require thinner wires which increases the parasitic inductance. An alternative I/O approach for 3D integration hangs the EIC off the edge of the PIC, where a high density glass ceramic interposer (GCIP) is used to provide a vertical connection from the MCM transceiver and the package substrate<sup>28</sup>. This allows for denser pitches and lower parasitics compared to wirebonds, with the tradeoff being assembly complexity.

For 2.5D integration, the PIC and EIC are both flipped onto an interposer, which provides the connectivity between the two dies with electrical traces. Common interposer materials include silicon, glass, and organic substrates. Data I/O from the MCM transceiver can be achieved with vias to the backside of the interposer—which interfaces to the package

substrate—or with bridges to interface between the MCM and another die or interposer. The bridge can be on top of two interposer tiles to provide connectivity<sup>29</sup> or embedded within an organic substrate, enabling trace densities beyond what may be supported by the organic substrate alone<sup>30</sup>. A common approach for implementing a vias is to use a thinned silicon interposer and create the connectivity between the front and back of the interposer using through silicon vias (TSVs). TSVs are often in the range of 100  $\mu$ m to 200  $\mu$ m tall, which makes it difficult to control the impedance of the TSVs. This impedance mismatch can introduce reflections, resulting in reduced signal strength and increased noise<sup>31</sup>. While it is difficult to control the impedance in TSVs, they can be design around—equivalent circuit models have been developed<sup>32</sup>, and transmission lines incorporating TSVs in the critical path have been demonstrated up to 50 GHz<sup>33</sup>.

More exotic alternatives to metal vias exist, such as the ThruChip Interface (TCI), which uses wireless connections through near-field inductive coupling<sup>34</sup>. The transmitter inductive coils produce a magnetic field through the silicon which is vertically received with a similar receiver coil. This approach offers a lower cost alternative to TSVs and has been demonstrated with 30 Gbps links<sup>35</sup>. A drawback of the TCI approach is the size of the coils—the diameter needs to be approximately three times the vertical distance transmitted<sup>36</sup>, for an aspect ratio of 1:3 (height to width). Comparatively, TSVs can be fabricated with an aspect of 10:1<sup>37</sup>, allowing for much denser pitches.

Whether vias through an interposer to the backside or a bridge on top of the interposer are used, the data I/O will often require fanout traces on the interposer. For high speed signals, these traces should be transmission lines to minimize impedance mismatch. Our 2.5D integrated MCM transceiver utilized a silicon interposer. Numerous types of transmission lines have been demonstrated in silicon interposers, including microstrip, coplanar waveguide, grounded coplanar waveguide, differential coplanar waveguide with good performance up to 50 GHz<sup>24,26</sup>. In developing the second generation of our MCM transceivers, three variations of 10 mm long transmission lines were investigated: a microstrip line using top level metal layers, a coplanar waveguide using the top metal layer, and a coplanar waveguide using the backside metal. For each variation, a transmission line was designed for 50 ohm impedance, as well as versions with slightly thicker and slightly thinner signal lines.



Figure 5. a) The model for two traces to simulate the interposer's transmission lines. b) The S parameters for the simulated interposer transmission line up to 30 GHz.

The top level microstrip transmission line was used in the MCM transceiver—the model used for simulation can be seen in figure 5 a). The performance of a differential pair can be seen in figure 5 b). The simulation shows that at 30 GHz S21/S12 is better than -1 dB and S11/S22 is less than -21 dB. While the performance of just the transmission lines on the interposer is expected to be good, it is necessary to include the bumps to the interposer in the simulation. For our MCM transceiver, 50  $\mu$ m diameter stud bumps were used between the EIC/PIC and interposer, and 300  $\mu$ m diameter BGA-type connections were used between the interposer and the PCB. The model used to simulate the interposer in HFSS can be seen in figure 6 a). Including these bumps in the simulation degraded the performance, as seen in figure 6 b). In the MCM transceiver, deserialization occurs in the EIC prior to fanout on the interposer, which results in a target data rate of 2.5 Gbps for the interposer transmission lines. Including the bumps at 2.5 GHz resulted in a S21/S12 of -1.2 dB, a S11 of -24.2, and a S22 of -13.3 dB for the simulated transmission lines.



Figure 6. a) The model in HFSS used to simulate the pair of transmission lines with the micro bumps and BGA-type solder balls included. b) The simulated S parameters up to 15 GHz.

#### 3.5 Design for Assembly

Designing the MCM transceiver to facilitate the assembly of the optical interface to the transceiver is a key component of the design process. For 2D and 3D integration, the integration with the EIC generally introduces minimal restrictions to optical coupling to the PIC. For 2D integration, the top area of the PIC is unaffected—with 3D integration, the EIC is flipped on top of the larger PIC, leaving top areas of the PIC uncovered. As a result, vertical coupling to grating couplers on the PIC is the most common optical coupling method in 2D and 3D MCM demonstrations<sup>24,26,38</sup>, though edge coupling has also been demonstrated<sup>39</sup>.

When implementing more complex integrations—such as 2.5D integration—the top area of the PIC may be mostly covered due to being flipped on top of an interposer. In this scenario, edge coupling is preferred approach, but can be challenging as most of the PIC's top is covered. To facilitate edge coupling to the PIC, one approach is to overhang the PIC off the edge by several hundred microns to a visual contact to the location of the edge coupler<sup>40</sup>. This approach was followed in developing our 2.5D MCM transceivers, as seen in figure X. While overhanging the PIC enables easier optical coupling, an alternative is to fabricate the interposer substrate with a trench to allow a fiber array to be coupled to the PIC in the middle of the MCM<sup>41</sup>. Another approach transforms the interposer to an optical interposer, which incorporates an optical waveguide layer to the interposer. With a silicon interposer, this optical waveguide can be implemented with a silicon nitride (SiN) layer<sup>42</sup>. Etching shallow trenches into the interposer enables the edge couplers of the flipped PIC to butt couple to the SiN waveguides in the interposer. The SiN waveguides can then route out to the edge of the interposer for conventional edge coupler fiber array attach. For integration requiring vertical optical routing through an interposer, optical TSVs have been developed, such as to allow a VCSEL output to route through an interposer to an optical printed circuit board<sup>43</sup>. The optical TSV can either be implemented with an air-filled TSV or a waveguide TSV. To design the waveguide TSV, the TSV needs to be coated with a low index material to shield the mode from the silicon that the TSV traverses<sup>44</sup>.

Similarly, designing the MCM transceiver with the electrical assembly process in mind can aid in ensuring that the prototype can be successfully assembled. One main consideration is the bump pitch for the PIC and EIC. Denser bump pitches allow for higher I/O counts, resulting in higher bandwidth densities. For bump pitches below 100  $\mu$ m, the most common approach is full wafer bump growth for both copper pillars and microsolder bumps. Full wafer bump growth may be acceptable for full transceiver development, but for smaller prototypes it may be too costly. While the standard for dense bump pitches is full wafer growth, some vendors do advertise single die bump growth as dense as 25  $\mu$ m<sup>45</sup>. For electrical I/O, the pitch limitations are dependent on the MCM substrate. While interposers support pitches comparable to those for EICs and PICs, PCBs are not able to be fabricated with as dense of pitches. Typical PCB fabrication minimums are three mil trace width and three mil trace spacing, which translates to a pitch of approximately 150  $\mu$ m. For our 2.5D integrated MCM transceiver, the backside of the interposer interfaced to a PCB with a BGA type

connection. Standard BGA packages can be supported with pitches down to 0.5 mm<sup>46</sup>—and we implemented our BGA type connections with 0.5 mm, as shown in figure 7 a). For our second iteration of prototypes, this dense BGA pitch made routing out on the PCB difficult, resulting in requiring a six-layer board and via-in-pads. A final consideration is bump reflow temperatures across a variety of bumps. For our MCM transceiver, we utilized stud bumps between the interposer and both the PIC and EIC, as shown in figure 7 b) along with the TSVs. The assembly order was PIC and EIC reflowed the interposer, and then interposer reflowed to the PCB. The reflow temperature of the stud bumps needed to be high enough that it would not reflow when the interposer was being attached to the PCB.



Figure 7. a) The PCB which interfaced to the backside of the interposer for the version 1 prototype for the MCM transceiver, shown with the BGA-type solder balls. b) An X-ray image of the interposer with the PIC and EICs flipped on top, taken prior to being placed on the PCB. The TSVs and stud bump solder balls can be seen in the image, as well as the PIC hanging off the interposer to facilitate optical coupling.

#### 4. CONCLUSION

In this paper, we provided an overview of our version 1 prototype operating at 7 Gbps. Additionally, we identified five areas of design with regard to developing silicon photonic MCM transceivers: integration architecture, equivalent circuit model development, PIC to EIC interface model development, MCM I/O design, and design for assembly. The process of developing the version 1 prototype helped identify the five design areas that were used to develop the version 2 prototype. Each of these design areas can impact the performance of the MCM transceiver, and if neglected can negate the potential benefits of introducing silicon photonics to data centers and high-performance computers.

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