3D-Integrated Multichip Module Transceiver for Terabit-Scale DWDM Interconnects

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Abstract: We present the architecture and assembly of a compact, 3D-integrated CMOS-silicon photonic transceiver for DWDM interconnects. The transceiver interleaves 64 parallel wavelength channels enabling energy efficient scaling of multi-Tbps/mm^2 bandwidth densities for future co-packaged chipsets. © 2021 The Author(s)

1. Introduction

Silicon photonic transceivers co-packaged with compute chips can provide an energy-efficient solution to the ever-growing bandwidth demands of distributed computing [1]. Such co-packaged transceivers must deliver high bandwidth in a low area to avoid parasitically fanning out the dense wiring of the package; the target bandwidth density for next generation interconnects is on the order of Tbps/mm^2 [2].

Here, we present the design and end-to-end assembly of a transceiver architecture that achieves an unprecedented bandwidth density. This design scales bandwidth across 64 parallel wavelength channels in a dense wavelength division multiplexing (DWDM) scheme afforded by a comb source [3]. On-chip filters are used to de-interleave and interleave wavelength channels into and out of transmitter and receiver banks. Modulators and photodiodes are combined with electronic drivers and receivers through dense 3D flip-chip bonding of a silicon photonic integrated circuit (PIC) and CMOS electronic integrated circuit (EIC), where copper pillar bumps allow a dense pad pitch of 25 μm. Furthermore, this approach has a straightforward path for scaling to mass production as both PIC and EIC are fabricated in multi-project wafer runs (MPWs) at commercial 300 mm facilities. The EIC in the demonstrated assembly was fabricated in a 180 nm CMOS process and is limited to data rates of 2 Gbps, however, the transceiver multi-chip module (MCM) capacity is designed to deliver a 5 Tbps/mm^2 bandwidth density at a per-channel data rate of 16 Gbps.

2. Transceiver Architecture

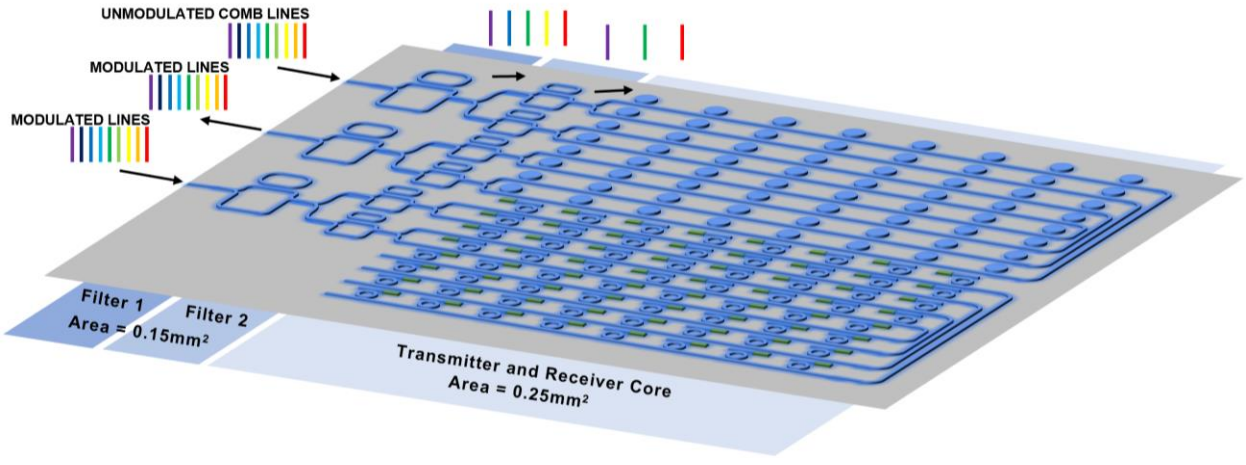

Fig. 1. Illustration of the transceiver PIC. Ring-assisted Mach-Zehnder interferometers (RMZIs) are shown in the Filter 1 and Filter 2 stages separating comb lines. Micro-disk modulators and micro-ring filters with photodiodes are shown in the north and south, respectively, of the Transmitter and Receiver Core.

2.1. Optical Path

The PIC is fabricated through the AIM Photonics MPW service. Figure 1. illustrates the optical paths through the PIC. Depletion-mode micro-disk modulators are the basic element of the transmitter, with each encoding data onto a single comb line. At the receiver, micro-ring filters are used to drop single modulated lines to germanium photodiodes. Micro-disk modulators, micro-ring filters, and germanium photodiodes are used from the AIM Process Design Kit [4]. Power hungry serialization and de-serialization at high data rates constrain per-channel bandwidth, and the sizable 127 µm cladding diameter of single mode fiber limits the number of optical I/O ports that can be included on a compact PIC transceiver. These factors necessitate highly parallel per-fiber wavelength multiplexing to maximize the bandwidth density. Unfortunately, cascading tens of modulators on a single bus for multiplexed channels results in unacceptable accumulated off-resonance insertion loss and large intermodulation crosstalk for small channel spacings. This PIC architecture overcomes these drawbacks by filtering lines on-chip from a single port into four buses of 16 cascaded modulators. Ring-assisted Mach-Zehnder interferometers (RMZIs) were selected as the filtering elements for their box-like spectral passbands and their compactness compared to other commonly used devices such as arrayed waveguide gratings. A single RMZI acts as a one-to-two de-interleaver, presenting passbands to even/odd channels in its upper/lower output ports. Two RMZI stages are cascaded to yield a one-to-four de-interleaver, quadrupling the bandwidth per I/O. The first stage RMZIs have a designed passband spacing of 300 GHz, while the second stage was designed with a 600 GHz spacing. The design of broadband RMZIs is described further in [5]. For the full transmitter circuit, 64 comb lines enter the PIC through an edge-coupler port, which are then split into 4 groups of 16 using cascaded RMZIs. Each comb line is then modulated by micro-disks on four separate bus waveguides, and are finally recombined by cascaded RMZIs to a single output port. The receiver splits 64 incoming modulated comb lines into 4 groups of 16 again using cascaded RMZIs, and receives each line with a micro-ring drop filter and photodiode. Modulators and photodiodes are spaced at a 25 µm x 75 µm pitch, as each has a data signal, data ground, and heater signal pad at a 25 µm pitch connected to the EIC. The full optical circuit fits within a 0.4 mm^2 area on the PIC.

2.2. 3D-Integrated CMOS EIC and Package Assembly

Modular cells on the EIC chip mirror the micro-disks and photodiodes on the PIC. Each EIC transmitter cell has a cyclical 16-bit data register loaded through a serial port. An external high-speed clock triggers all transmitter data registers and single-ended drivers switch micro-disk modulators on the PIC. The receiver cells convert current from the photodiode on the PIC to voltage using transimpedance amplifiers and store data in a register to be read out using a serial port. EIC transmitter and receiver cells are equipped with heater DACs for thermally tuning the modulator and micro-ring filter resonances against fabrication offsets and ambient temperature fluctuations. The EIC was fabricated using the TSMC 180 nm CMOS process node; although the node size limits the designed data rate to 2 Gbps, it enables a cost-effective and quick-turn prototyping of dense 3D integration. An EIC based on the TSMC 28nm CMOS process is currently in development and is projected to achieve per-channel data rates up to 16 Gbps. The EIC is 1.5 mm x 1.5 mm with all transmitter and receiver cells only occupying 0.25 mm^2. Figure 2a. shows an optical microscopic image of the fabricated EIC die.

Figure 2. presents the end-to-end assembly of the transceiver. The PIC and EIC from foundry MPWs are received as singulated dies which are not amenable to dense copper pillar fabrication. To emulate the wafer-level bumping process, the EIC is placed in a molded plastic carrier wafer. Next, the aluminum-terminated pads of both dies are plated with under-bump metallization, followed by solder-tipped copper pillar fabrication on the EIC pads (Figure 2b). The EIC is then diced out of its carrier and flipped against the PIC for pad-to-pad bonding.

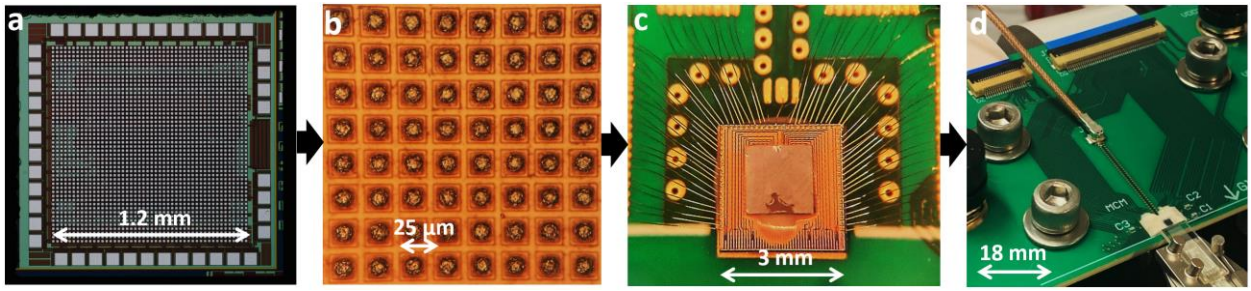

Fig. 2. Transceiver assembly flow. (a-c) Optical microscope image of: (a) the EIC before post-processing, (b) EIC pads with solder-tipped copper pillars fabricated, (c) PIC with EIC flipped on top and wire-bonded to PCB. (d) Transceiver on PCB with glob-top over wire-bonds and fiber array coupled to PIC.

The combined EIC and PIC multichip module is then attached and wire-bonded to an evaluation PCB (Figure 2c). Power, signals, and controls are fed through the wire-bonds to the PIC, and then to the EIC via metal layers on the PIC. A protective glob-top is cured over the wire-bonds and is dammed on the side of the PIC with edge couplers to allow for fiber array coupling with a micro-positioner (Figure 2d).

3. Results

Figure 3. shows the aligned spectra of the cascaded RMZI stages. On-chip evanescent taps were placed between RMZI stages to isolate and thermally tune the spectrum of each stage. An OSA was used to scan isolated RMZI spectra, while doped silicon heaters were used to thermally tune the optical path length of the ring and delay arm for each RMZI. Figure 3b. is the resulting aligned spectrum through both stages for one of the four buses. The cascaded spectrum has passbands with a 5.2 nm (650 GHz) spacing and a worst-case extinction ratio of 12 dB. To the best of the authors' knowledge, this is the most compact demonstration of cascaded RMZI stages with an area of 0.05 mm^2. The EIC was powered on, but low bump yield between PIC and EIC in the current iteration has prevented showing data transmission here.

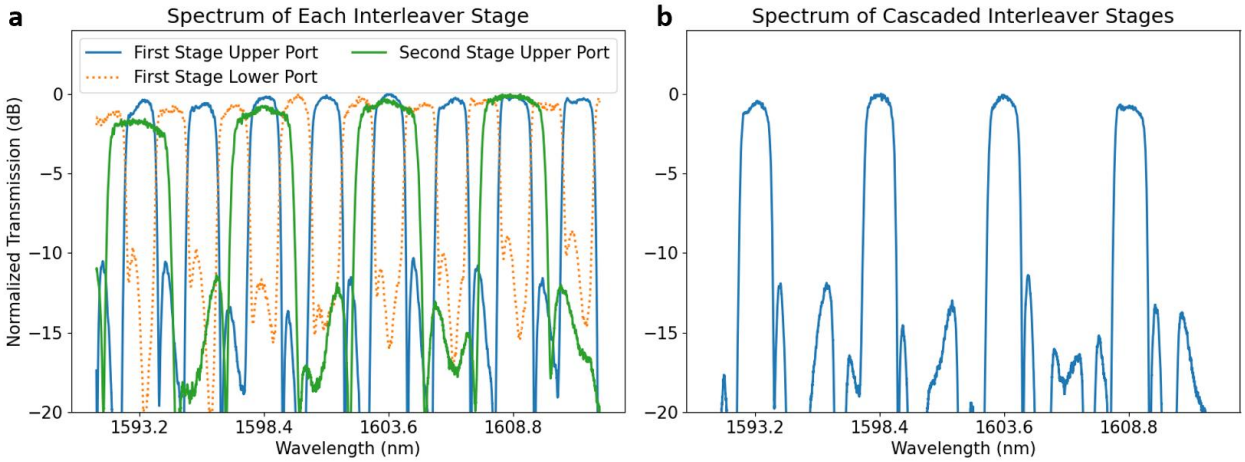

Fig 3. RMZI interleaver spectra. (a) First and second stage isolated and aligned spectra. (b) Spectrum through cascaded RMZIs leading to a single bus.

4. Conclusion

The design, architecture, and assembly of an ultra-compact 3D-integrated MCM transceiver was described and demonstrated with the potential for extreme bandwidth densities on the order of multi-Tbps/mm^2. Dense copper pillar connections between the PIC and EIC enable low footprint transmitter and receiver banks, and compact filtering is achieved with cascaded RMZI interleaver stages. The proposed transceiver architecture demonstrates a clear path to achieving multi-Terabit/s/mm^2 interconnection bandwidth densities between dense chip packages.

Acknowledgements

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