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Mitigation of parasitic junction formation in compact resonant modulators with doped silicon heaters

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ABSTRACT

While the high index contrast between silicon and silicon dioxide in the silicon-on-insulator photonics platform permits unprecedented device density, it also leads to high sensitivity to fabrication variations. In silicon microring and microdisk resonator devices, fabrication variations can substantially change the target resonance wavelength. Silicon's high thermo-optic coefficient allows for correction of these fabrication variations and stabilization of the device resonant wavelength through thermal tuning. Metal and doped silicon integrated heaters are commonly used to perform this tuning and have become an essential feature of silicon microring and microdisk modulators. Metal heaters are typically placed in a layer above the silicon devices, while doped silicon heaters are placed in the same silicon waveguide layer, adjacent to the devices. The advantage of doped silicon heaters over metal heaters is increased efficiency due to closer proximity to the optical device. However, for active devices using p-n junctions such as modulators, parasitic diode junctions can form between the doped heater and the modulator junctions, resulting in highly unstable and substandard device performance. Here, we present a detailed simulation framework for heater design in resonant silicon microdisk modulators, supported by experimentally measured device performance, which emphasizes tuning efficiency while eliminating parasitic diode formation. Simulations were conducted in Ansys Lumerical HEAT, CHARGE, and MODE to model parasitic junction behavior between the heater and modulator, in addition to the heater's thermal response and its effect on the resonant wavelength of the microdisk.

Keywords: Silicon Photonics, Resonant Modulators, Integrated Heater Design

1. INTRODUCTION

As the digital world continues to expand at an exponential rate, the current interconnect infrastructure in hyper-scale data centers and high performance computers is facing fundamental physical limitations to further scaling. Compounding the problem, modern workloads such as deep learning are highly computationally intensive and have serious environmental and economic consequences even at their current scale.[1] Thus, to keep pace with growing bandwidth demands while simultaneously reducing energy consumption, the introduction of co-packaged optical interconnects which transfer data via light rather than electrical signaling will become a necessity in the near future.[2–6] In particular, silicon photonics is well-suited for co-packaged optics solutions due to its compatibility with standard complementary metal-oxide-semiconductor (CMOS) fabrication and packaging infrastructure[7,8] as well as its natural support of single-mode dense wavelength-division multiplexing (DWDM) with resonant devices.[9] Many recent demonstrations from academia and industry have shown extremely high bandwidth data transmission with low energy-per-bit through leveraging DWDM with optical frequency comb sources and compact silicon photonic chips,[10–16] showing a promising path for future energy-efficient optical interconnects with unprecedented bandwidths.

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Resonant devices, such as microring and microdisk resonators, play an essential role in such DWDM links due to their small footprint, wavelength selectivity, and versatility in applications ranging from optical frequency comb generation[17] to modulation[18,19] and filtering.[20] The high refractive index contrast between silicon and SiO_2 in the silicon-on-insulator (SOI) platform allows for minimal bend radiation loss for extremely small bend radii down to a few micron, and the fully etched outer wall in microdisk cavities allows for extreme confinement of the whispering gallery mode with negligible bend loss compared to ring cavities with partial-etched outer walls required to form electrical contacts.[18,21] While the high index contrast in the SOI platform enables extremely small footprint devices, it also leads to a high sensitivity to nanometer-scale variations in the device geometry from fabrication variations. For resonant devices, this perturbation to the effective refractive index of the cavity path results in a shift of the resonant wavelength and thus requires correction to align the non-ideal wavelengths with the desired DWDM grid.

Tuning photonic devices via silicon's strong thermo-optic effect ($\frac{dn}{dT} = 1.8 \times 10^{-4}$ K^{-1}) has become the most common method of correcting fabrication-induced phase errors. Thermal tuning with an integrated heater is an essential component of silicon microring and microdisk resonators, as it is necessary to correct the resonant wavelength for both fabrication variations and thermal fluctuations. The two predominant categories of integrated heaters are:[22] (i) metal resistors formed in a layer typically above the silicon waveguide, and (ii) doped silicon resistors formed in the same plane as the silicon waveguide layer. While doped silicon heaters can be placed in closer proximity to the optical mode and thus achieve higher efficiencies, since they are formed in the same silicon layer as the device itself, they can lead to the formation of parasitic junctions (e.g. p-i-p and p-i-n) with neighboring contacts used for electro-optic modulation. State-of-the-art resonant modulators from literature[19,21] suffer from these parasitic diodes due to their small radii (10 μm and 3 μm, respectively) and lack of isolation between the heater and modulating p-n junction besides intrinsic silicon. While the width of the intrinsic silicon can be engineered to ensure that the parasitic diodes do not turn on under normal operating conditions, foundry design rules, dopant diffusion, and physical space limitations prevent full isolation for small footprint cavities and increasing the device size is highly undesirable due to the corresponding decrease in free spectral range (FSR) and increase in series resistance.

In this work, we present simulation models of custom designed silicon microdisk modulators with fully isolated integrated doped silicon heaters using the Ansys Lumerical suite and verify the results using devices fabricated at a 300 mm commercial foundry. We find excellent agreement between our simulated models and experimental measurements in terms of both thermo-optic efficiency and current-voltage characteristics. Notably, we show that for compact devices where the doped silicon heater is separated from an adjacent contact by only intrinsic silicon, a 100 nm oxide isolation barrier analogous to shallow trench isolation (STI) in microelectronics is fully resolved by the lithography and provides full electrical isolation between the heater and adjacent contacts while only sacrificing 7% of tuning efficiency. The demonstrated heater design methodology will enable more reliable and robust resonant modulators for future co-packaged DWDM silicon photonic interconnects.

2. DEVICE DESIGN

Microdisk modulators offer myriad features beyond standard microring modulators, including a larger free spectral range, higher modulation efficiency, and lower power consumption.[23] Since the traveling wave cavity supports a whispering gallery mode with low radiation loss due to the lack of an internal boundary condition, extremely small resonators can be realized, which drastically increases the free spectral range and greatly decreases the parasitic resistance and capacitance. Furthermore, the mode profile naturally supports a vertical junction with internal contacts[18,21] which has better overlap between the depletion region and optical mode and thus has a larger modulation efficiency than lateral junction designs, enabling operation at CMOS-compatible drive voltages (below 1 V).

In our microdisk design, the doped modulator contacts are required to be in close proximity to the doped silicon heater since they both reside on the interior of the compact 4.5 μm radius disk. The heater is a 5.9 x 0.6 μm rectangle of doped silicon within the center of the disk, while the highly doped silicon modulator contacts are semicircles on either side of the rectangular heater's long edge.[21] When the doped heater and modulator junctions reside in the same layer and in close proximity, parasitic currents can hinder the device performance. In order to mitigate the problems associated with significant currents between the heater and the modulator

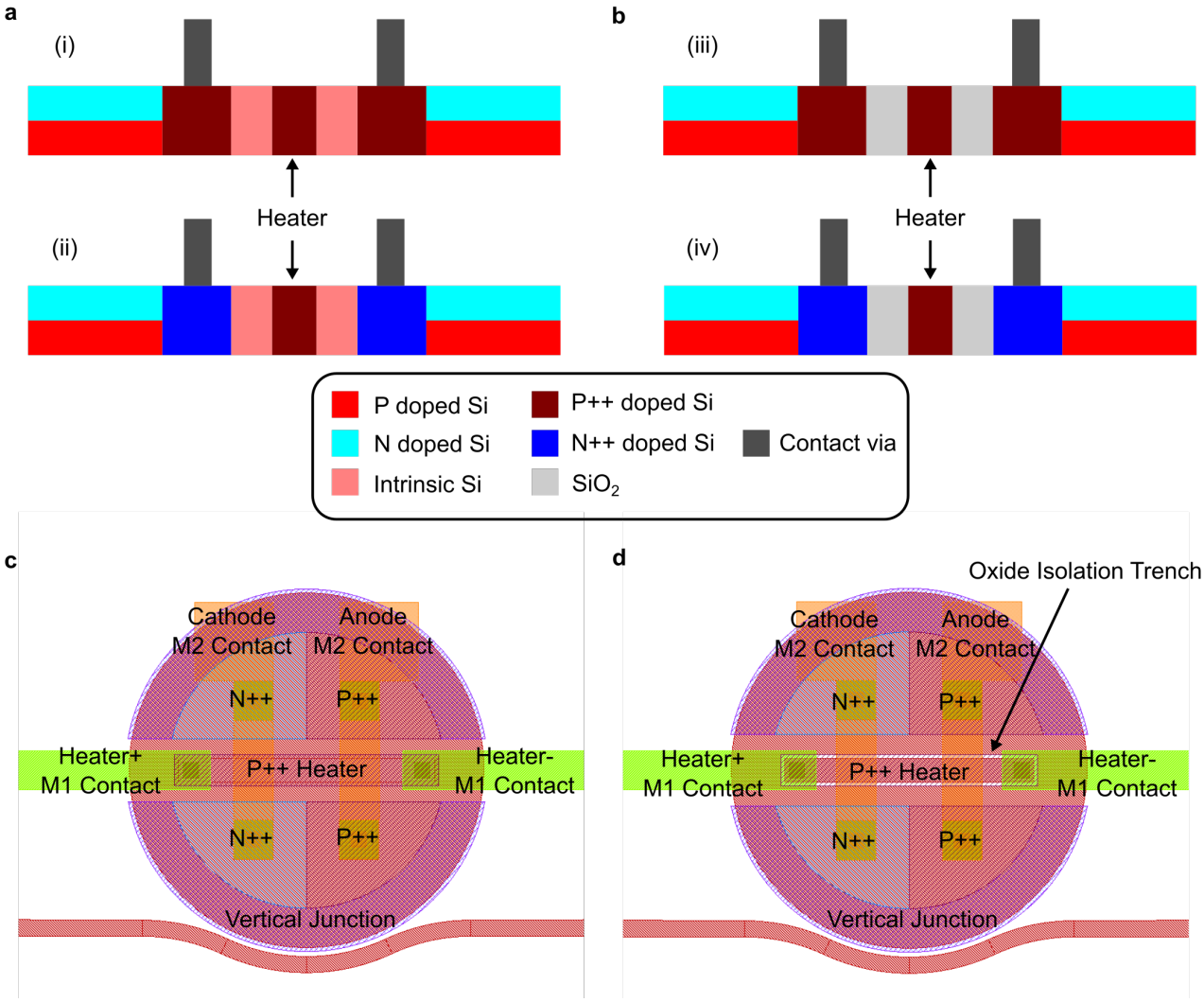

Figure 1. **a,** Cross sectional view of the microdisk modulator without oxide isolation trench where (i) is the cross section for the P doped contact and (ii) is the cross section for the N doped contact. The thin strips of intrinsic silicon separating the heater from the junction contacts give rise to parasitic diodes. **b,** Cross sectional view of the microdisk modulator with oxide isolation trench where (iii) is the cross section for the P doped contact and (iv) is the cross section for the N doped contact. The thin strips of intrinsic silicon are etched and replaced with oxide to electrically isolate the heater from the junction. **c,** Top view layout of the disk without oxide barrier for fabrication. **d,** Top view layout of the disk with oxide barrier.

junction arising from these parasitic junctions, we add an oxide barrier, of minimum thickness for the process DRC, surrounding the heater to achieve complete electrical isolation between the two elements (Fig. 1).

3. MICRODISK HEATER SIMULATION

3.1 Oxide Barrier

To capture the full electrical and electro-optic behavior of various heater designs with and without an oxide isolation trench, we perform simulations in the Ansys Lumerical environment.[24,25] Carrier dynamics and heat transport simulations are performed using Lumerical's finite element TCAD tools, and the generated carrier and temperature profiles are then exported to finite difference optical solvers (MODE and FDTD) to evaluate the

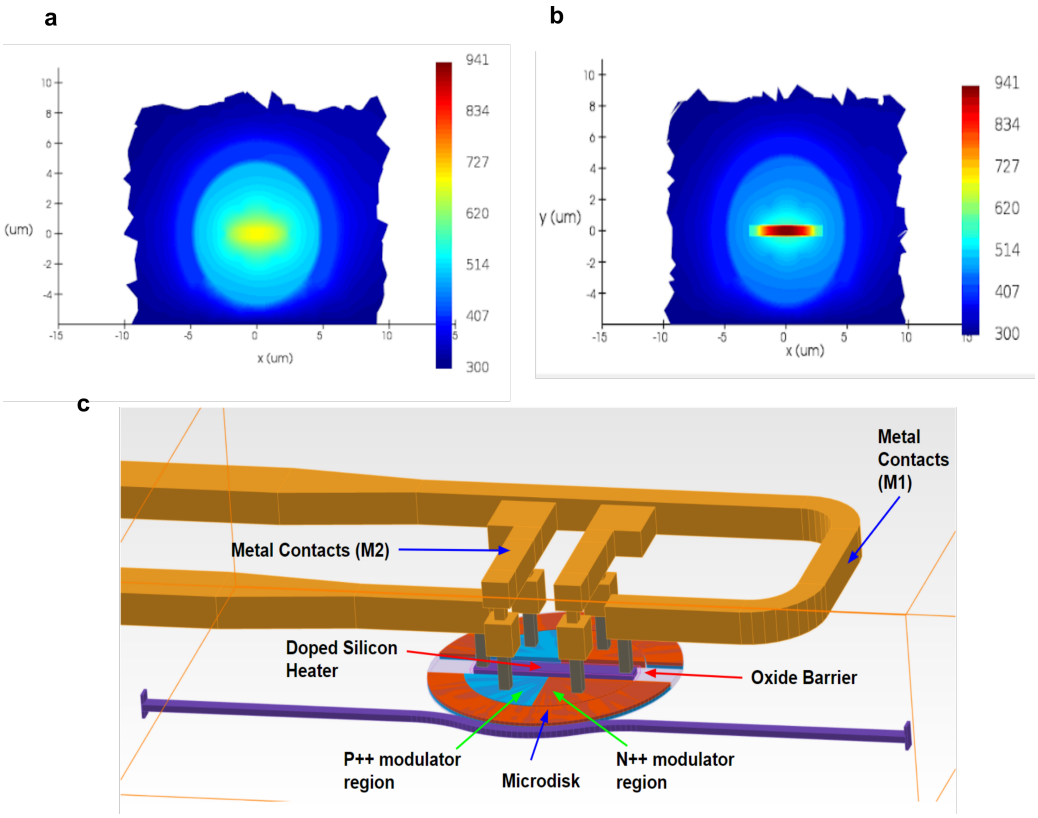

Figure 2. **a,** Thermal map of microdisk with 5V applied to the heater, without oxide barrier **b,** Thermal map of microdisk with 5V applied to the heater, with oxide barrier **c,** CAD simulation model of microdisk within the Lumerical environment.

combined performance. The TCAD simulation model is shown in Fig. 2 along with simulated heat maps for a 5 V bias across the heater terminals, with and without an oxide isolation trench.

From electrical simulations of the full structure without an oxide isolation trench, it is clear that significant current flows through the junction anode and cathode when only the heater is biased due to the parasitic junctions that form. Fig. 3a shows the equivalent circuit of the full modulator system with the parasitic connections that form between the heater and junction. Fig. 3b plots the simulated currents through each port when the heater is biased with all other nodes grounded, showing that significant diverging current flows through the modulator cathode once the parasitic diode turns on around 1 V. From Fig. 3c, the equivalent circuit for the oxide barrier device consists of two uncoupled circuits due to the full electrical isolation between the heater and modulating junction. The simulated performance in Fig. 3d confirms that the two circuits are fully isolated since biasing the heater does not induce any stray current to flow through the modulator anode/cathode.

Fig. 4 plots the heater efficiency for different heater dimensions for both designs with and without oxide isolation trenches. To generate the plots, cross sectional temperature maps for each case were exported as a function of applied heater bias and imported into Ansys Lumerical MODE for optical simulation. The finite element temperature grid is placed over the silicon disk cross section and the refractive index perturbation is calculated using silicon's thermo-optic coefficient ($\frac{dn}{dT} = 1.8 \times 10^{-4}$ K^{-1}). The solver then calculates the optical whispering gallery mode from the disk cross section and bend radius in cylindrical coordinates, providing the change in effective index as a function of heater bias. Finally, the effective and group indices for each bias condition are imported into an S-parameter-based circuit simulator (Ansys Lumerical INTERCONNECT) to calculate the shift of resonance with applied bias. While the full 3D heat map could be exported to a 3D FDTD simulation to simulate the full structure, high quality factor optical resonators are extremely computationally expensive to simulate in the time domain since simulation convergence is based on field decay. Despite using a cross sectional

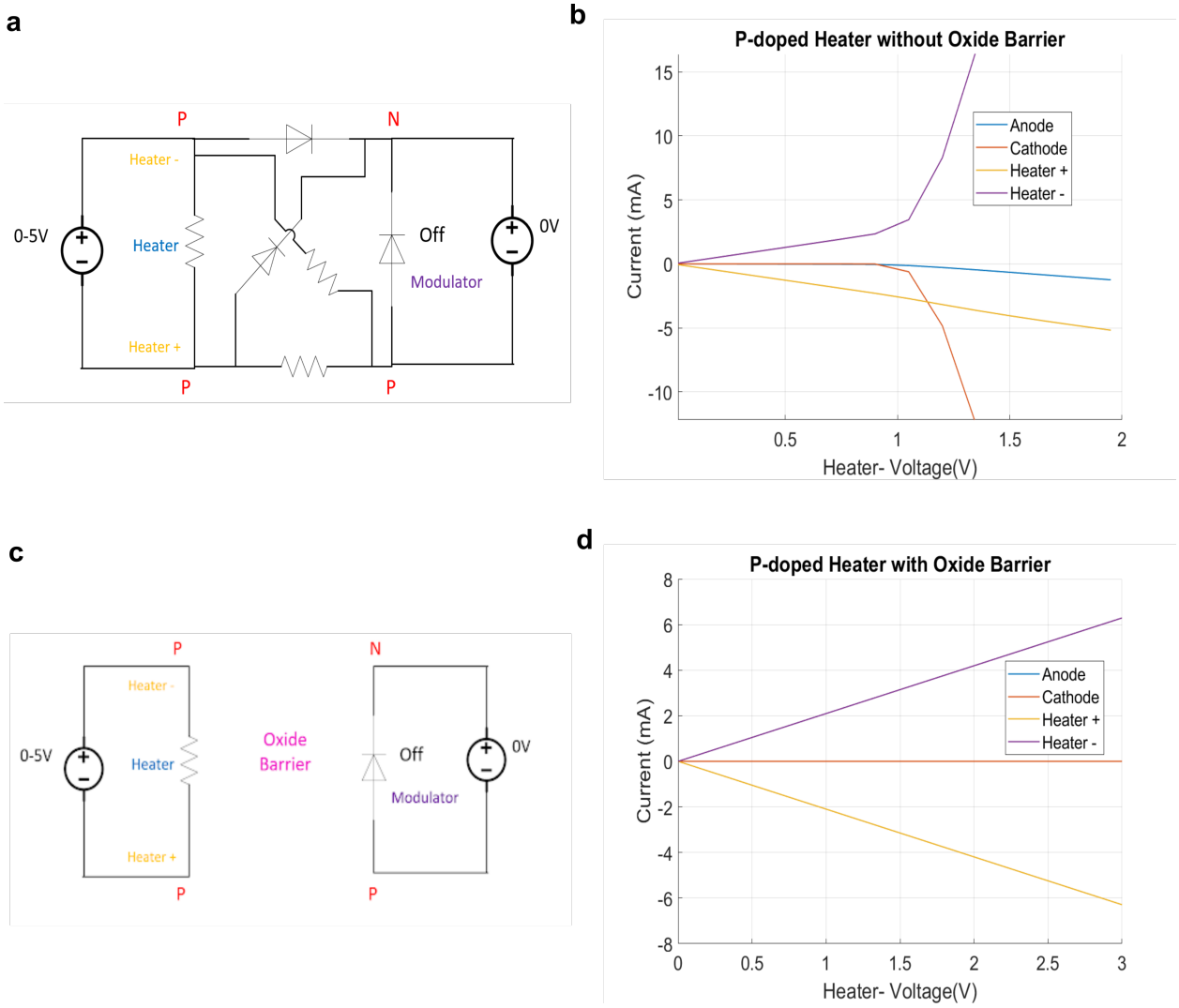

Figure 3. **a,** Microdisk circuit model for p++ doped heater, without oxide barrier, no modulation. **b,** Lumerical simulation current plot at four ports for Heater- sweep 0-5V, without oxide barrier, no modulation. **c,** Microdisk circuit model for p++ doped heater, with oxide barrier, no modulation. **d,** Lumerical simulation current plot at four ports for Heater- sweep 0-5V, with oxide barrier, no modulation.

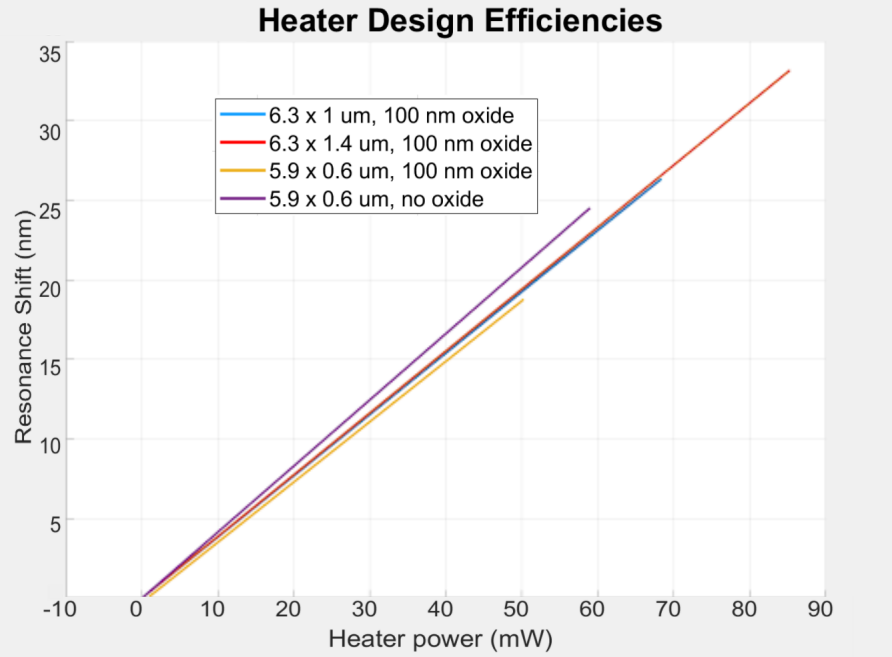

Figure 4. Microdisk resonance shift versus heater power simulation of different sized heaters with and without 100 nm oxide barrier.

2.5D approach for the thermo-optic simulations, in Sec. 4 we show that our simulated thermal efficiencies closely match measured experimental results. The efficiency for a heater of identical dimensions minimally decreases with the addition of an oxide barrier, displaying a tuning efficiency of 0.36 nm/mW (0.096 rad/mW) with an oxide barrier versus 0.42 nm/mW (0.11 rad/mW) without an oxide barrier. Thus, our simulations indicate that introducing a narrow oxide isolation trench is a viable solution for removing parasitic currents in the microdisk modulator without severely impacting the efficiency.

3.2 Selective Substrate Undercut

From Fig. 4, we observe that with a $\approx 14\%$ decrease in efficiency we can eliminate the unstable parasitic junction. However, by selectively removing the substrate beneath the device, the efficiency for devices both with and without an oxide barrier can be greatly increased by over $20\times$.[22,26–28] The substrate provides the path of lowest thermal resistance away from the integrated heater and thus replacing the silicon substrate with air thermally isolates the device, greatly confining the generated heat. To model the effects of a substrate undercut on our microdisk modulators, we perform simulations in Lumerical HEAT similar to those detailed in Sec. 3.1. Fig. 5a compares simulated resonance shifts as a function of dissipated heater power for the undercut and non-undercut designs, showing a drastic increase in efficiency for the undercut heater. Since the efficiency is increased by over $20\times$, using an undercut will make the efficiency decrease from the oxide isolation trench effectively negligible since the magnitude of the percent difference between oxide and no oxide designs will be decreased by $20\times$. While the use of a substrate undercut is highly appealing from an efficiency perspective, since the device is more thermally isolated, an undercut also results in reduced rise and fall times for the device heater response. Fig. 5b shows the difference in time to reach steady state temperature between the undercut and non-undercut case, displaying a large increase in rise time for the undercut device. However, since the device is also better isolated from ambient thermal fluctuations, the resulting decrease in modulation bandwidth for the undercut microdisk should not significantly affect the ability of the thermal control circuitry to compensate for resonance drift.

We have recently demonstrated a wafer-scale-compatible selective substrate undercut in the AIM Photonics 300 mm platform with minimal post-processing steps and showed an ultra-efficient doped silicon thermal phase

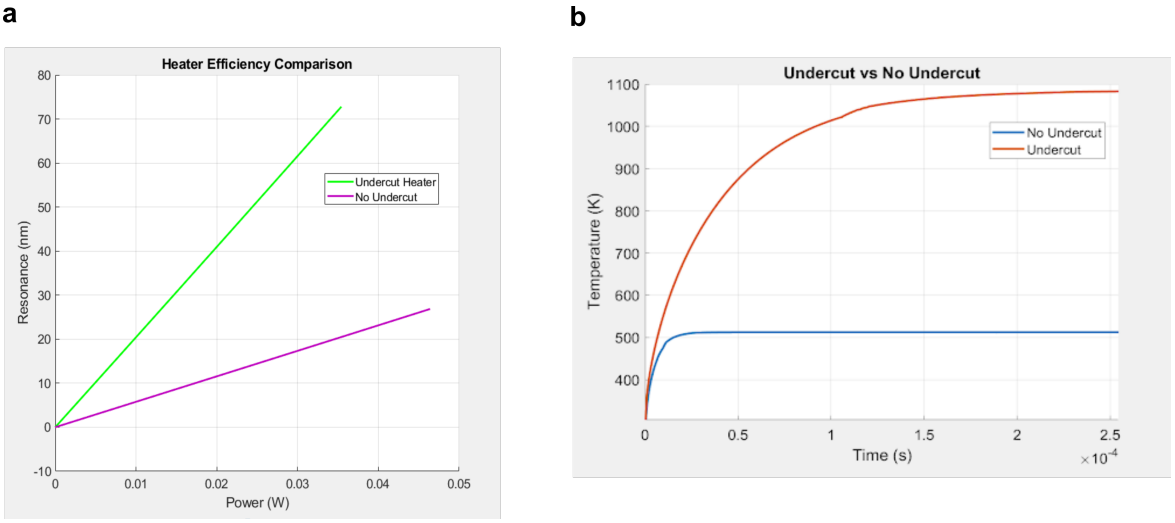

Figure 5. **a,** Heater efficiency simulation comparison with (green) and without (pink) undercut structures **b,** Transient temperature simulation comparison with (red) and without (blue) undercut structure

shifter with $P_\pi = 1.2$ mW (2.62 rad/mW).[29] Process development with the foundry is on-going to eliminate all post-processing steps and enable undercut devices fabricated entirely at the wafer scale. Furthermore, we have taped out extensive design-of-experiment undercut microdisk modulators on a recent dedicated wafer run to fully explore trade-offs of the undercut geometry. We expect these experiments and process development to enable large-scale resonator circuits with hundreds to thousands of ultra-efficient undercut microdisk modulators on a single chip.

4. EXPERIMENTAL RESULTS

To validate the simulated device performance, we designed and taped out various microdisk modulator test structures including devices with oxide isolation trenches ranging from 100 nm to 300 nm and a control group without isolation trenches. The silicon photonic chips were fabricated through a private 300 mm dedicated wafer run with AIM Photonics/SUNY CNSE.[30] Fig. 6 shows optical microscope images of the representative microdisk modulator designs with and without an oxide isolation trench.

Lensed fiber was used to couple light onto and off of the chip through inverse-tapered edge couplers. A tunable laser was swept at the input of the chip with a triggered power detector at the output to measure the spectrum of each microdisk. Multi-contact DC wedge probes at 100 μm pitch were used to electrically connect to each device and a programmable source-meter was used to provide biases and measure currents on each pin. Fig. 7a shows the measured spectrum for a single FSR and Fig. 7b shows the shift of resonance as a function of applied heater bias up to 5 V.

Fig. 8 shows experimental current measurements at the anode, cathode, heater+, and heater- ports. Figs. 8a and 8b display current for a disk without a heater oxide barrier, while Figs. 8c and 8d show current for a disk with the heater oxide barrier. The measurement sweeps match the simulation results closely, and the currents reach approximately the same values as they do in the heater simulations before the source-meter saturates in current. As observed in simulation and experiment, the absence of an oxide barrier contributes a considerable amount of excess current between the heater and junction. This large unwanted current flowing through the junction additionally interacts with the optical mode, resulting in high loss from free-carrier absorption and thus a greatly degraded quality factor.

Figure 9 plots a comparison of measured heater efficiencies with and without an oxide barrier. The efficiency for the heater with an oxide barrier is only slightly lower than the heater without the barrier. The microdisk with the oxide barrier exhibits a measured efficiency of 0.37 nm/mW (0.099 rad/mW) compared to 0.4 nm/mW

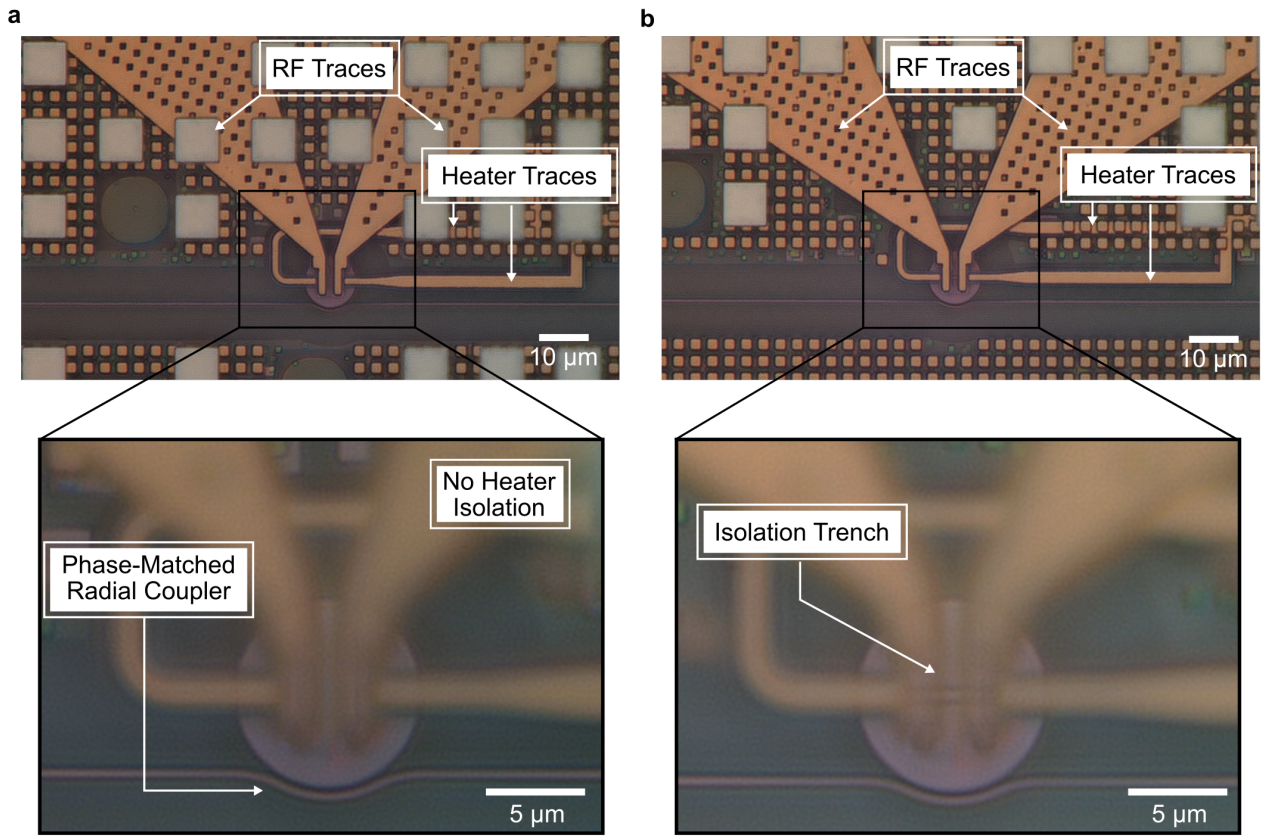

Figure 6. **a,** Optical microscope image of the nominal microdisk modulator without an isolated heater. The zoomed view shows the radial coupler phase-matched to selectively excite the fundamental TE whispering gallery mode of the disk. **b,** Optical microscope image of the microdisk modulator with a 100 nm wide oxide isolation trench surrounding the heater. The zoomed view highlights the narrow isolation trench surrounding the heater, which is clearly visible at 6,000× magnification but is blurry due to the trench critical dimensions being close to the diffraction limit for visible light. Future validation of the etch dimensions will be done using scanning electron microscope imaging.

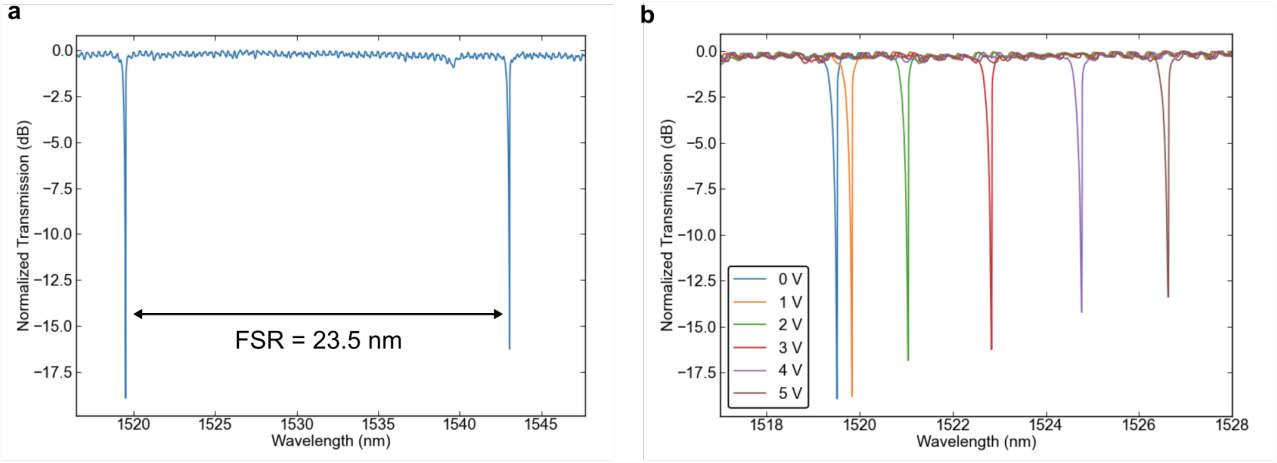

Figure 7. **a,** Experimentally measured FSR of the fabricated device showing near-critical coupling with no presence of higher order modes. **b,** Experimentally measured thermal tuning as a function of voltage for a representative device with an oxide isolation trench.

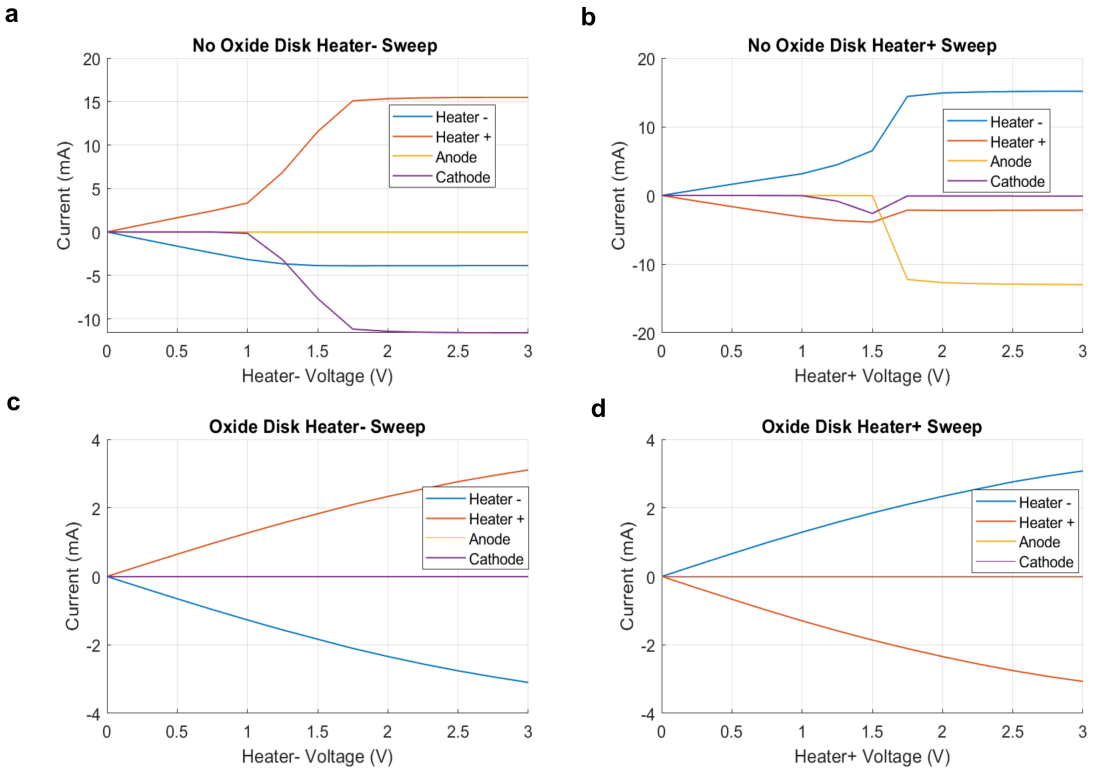

Figure 8. Experimentally measured microdisk IV curves from heater voltage sweeps, with and without oxide barrier, all ports apart from Heater- at 0V: **a,** No oxide, heater- swept. **b,** No oxide, heater+ swept. **c,** Oxide, heater- swept. **d,** Oxide, heater+ swept.

(0.107 rad/mW) without the oxide barrier. These experimentally measured results closely match simulation, validating our modeling framework. From this data, we conclude that the oxide barrier has minimal adverse effect on the efficiency of the heater while providing protection from extraneous currents that occur between the parasitic junctions of the doped silicon heater and the modulator junctions.

5. CONCLUSION

Resonant modulators have proven to be an essential building block for future silicon photonic systems due to their compact footprint, high bandwidth, and low energy consumption. Microdisk modulators, through high confinement of the optical mode, enable tremendously small footprint devices with radii below 3 μm, which presents a significant challenge in the design of an integrated heater. In this work, we have proposed a simulation framework, through which we have demonstrated a photonic equivalent to shallow trench isolation to electrically isolate the internal doped silicon heater from the rest of the disk while maintaining close proximity to the optical mode. From corresponding simulated and experimentally measured results, we verified that this narrow oxide isolation trench minimally decreases the heater's thermo-optic efficiency (7% decrease) while also providing full electrical isolation from the p-n junction used for electro-optic modulation. Through simulations, we have also investigated the impact of selective substrate undercuts on the device's thermo-optic efficiency, showing that the degradation in P_π from the isolation trench can be made nearly negligible if such an undercut is implemented. To verify these simulated undercut results, we recently taped out a dedicated 300 mm wafer through AIM Photonics with various wafer-scale undercut microdisk modulator test structures which is expected back for measurements in Q2 of 2022. We expect the demonstrated heater architecture to significantly increase the reliability and performance of microdisk modulator-based DWDM silicon photonic interconnects in future data center and high performance computing systems.

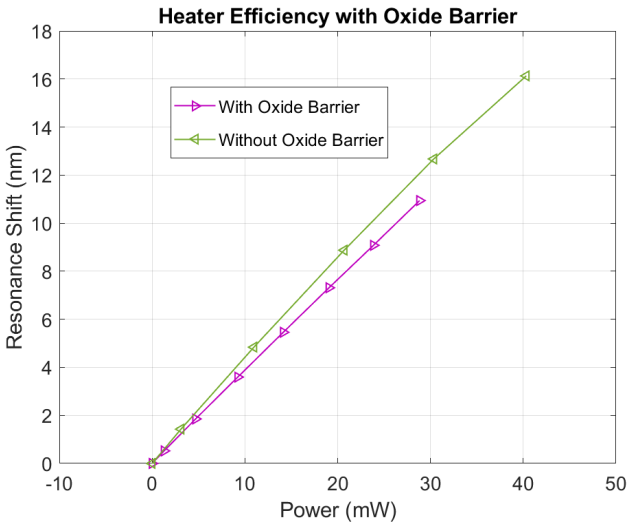

Figure 9. Experimentally measured heater efficiency with oxide barrier (pink) and without oxide barrier (green).

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