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Package Design and Measurements for Radar Emulator using Accelerators and Photonics

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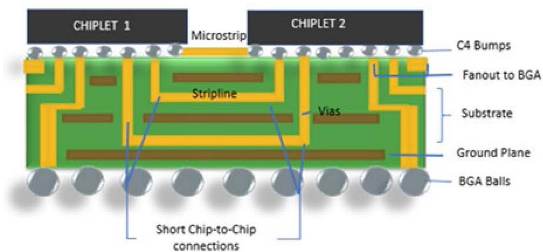
Abstract—Real-time radar emulators require high-speed computing operations where large amounts of data need to be stored and processed. This requires a high-speed computer architecture consisting of multiple CPU nodes networked to each other through optical fibers, to ensure that each node can communicate with every other node. Each CPU node consists of an accelerator IC (ACC) for matrix multiplications and multiple photonic ICs (PIC) for data transmission. The focus of this paper is on the electrical characterization of interconnects in an organic package that establishes communication between the ACC and PIC at a speed of 16 Gbps.

Custom integration of photonics with electronics in a single module is required for supporting the required bandwidth, speed, and energy efficiency. In this paper, we explore several variations of the interconnect technology placing emphasis on the importance of impedance matching between the electronic drivers and the photonic modulators. To enable the implementation of these interconnects we have designed a test vehicle (TV) with varying topologies for electrical characterization up to 110 GHz. In addition to the design, this paper presents the characterization of interconnects in the fabricated TV, of varying impedances, lengths, and spacing on multilayer organic substrates with very low loss-high frequency dielectric materials. The losses are characterized up to 110 GHz for microstrip lines, striplines, vias, microstrip, and ring resonators, along with a full channel characterization with an impedance range of 50 ~ 80 Ohm and short interconnect lengths in the range 1 ~ 5 mm, respectively. This paper includes model to hardware correlation studies.

Keywords—Radar, Heterogeneous Integration, Photonics, Organic Interposer, Loss, VNA Measurements

I. INTRODUCTION

High-speed computing operations with custom chips have a wide range of applications where for example networked systems can support large data transmission rates between processing nodes. Typical transmission rates are on the increase[1][2], and in response interconnect standards are on the rise, especially to support heterogeneous integration platforms. New packaging technologies help drive heterogeneous integration (HI) which allows the portability of custom technology nodes also known as "chiplets" assembled onto advanced packaging platforms, as shown in Figure 1. In [3], the AMD EPYC processor uses the chiplet technology for a DDR4 channel, with a reported ~23.5 Gb/s peak bandwidth on an organic substrate. Low loss and high bandwidth interconnects are the key components for realizing high-speed signal transmission between integrated circuits in chiplets[4]. While popular interconnect standards such as Intel's Advanced Interface Bus (AIB) have attempted to define minimum parameters such as eye width 0.1UI – 0.2UI, 0.85 pJ per bit, and 0.06 ns delay for the channel link [5], including others such as JESD204C for 32 Gbps for HPC applications[6], many more are emerging such as the UCIe (Universal Chiplet Interconnect express) where the key factors driving the standards are the I/O link performance[2], power consumption(pJ/bit), and loss(dB/mm).



To achieve the high speeds needed for supporting radar emulator applications, tight integration between the photonics and electronic circuits on a package that establishes a direct connection between the driver output and modulator input is needed. As shown in Figure 1, interconnect lines need to be kept as direct and short as possible to increase I/O density and reduce signal parasitics. Increasing the I/O link bandwidth implies scaling the density of all components in the physical channels i.e. microstrip, bumps, vias, etc. [2]. However, in scaling, there are size constraints for HPC applications that require significantly reduced dimensions and several investigations into the limits of the interconnect performance for high-density chip-to-chip communication.

Silicon interposers have a reticle size constraint of 26 mm x 32 mm in both prototyping and manufacturing, which establishes constraints since the ACC used in radar emulators such as the one addressed in this paper have large dimensions (e.g., 25 mm x 25 mm) and need to be connected to the PIC on the same substrate,

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making the substrate sizes much larger. Organic laminates, an established technology provides opportunities here for supporting larger substrate sizes, provided new materials can be integrated into the substrate for supporting both high density and low loss connections, for managing signal integrity.

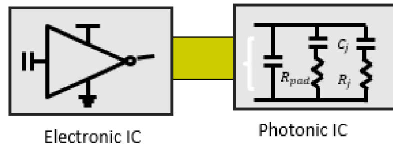


Figure 2. Photonic – Electronic Single-Ended Connection.

The communication between the Electronic IC (EIC) in the ACC and PIC needs to be established through the substrate connections, as shown in Figure 2. This requires a combination of interconnect structures in the substrate, as shown in Figure 3 such as microstrip, striplines, vias, and transitions with their related parameters as defined in Table II.

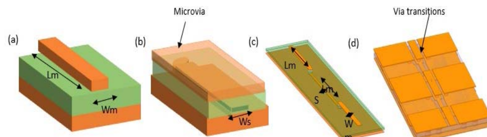


Figure 3. Interconnect structures (a) microstrip (b) stripline (c) microstrip-stripline transition (d) daisy chain transitions.

II. PACKAGE SUBSTRATE DESIGN

Signal degradation in the channel needs to be addressed for high-frequency transmission, which includes cross-talk isolation, impedance management, insertion loss, matching, supply inductance, and manufacturing-related non-uniformities. The communication path being targeted in this paper is shown in Figure 4, where the interconnects are in the package substrate.

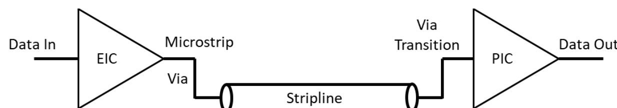
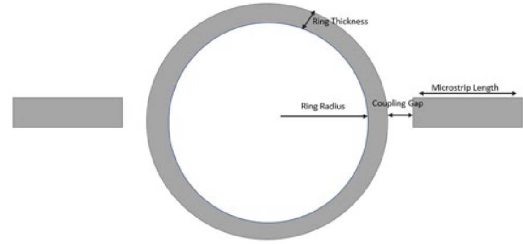


Figure 4. Communication path causing channel degradation [8].

Scattering (S) parameters can be used in the frequency domain to appropriately capture the amplitude, and phase response of interconnect structures. The S parameters can then be used as a black-box model to cascade individual blocks for computing the full channel loss.

To properly characterize the interconnect structures we characterize the organic substrate using a Microstrip Ring as shown in Figure 5, to extract the dielectric behavior over high frequencies. A microstrip ring resonator works by coupling the signal from the microstrip line to the ring, which can be used to extract the material permittivity. To design the microstrip ring resonator, equation 1 was used where fn is the nth resonant frequency, c is the speed of light, ε_{eff} is the effective dielectric constant, and rs is the mean radius of the ring. After design and measurement, the extracted response at specific frequencies (f_n) is used to estimate the dielectric constant of the material.

$$f_n = \frac{nc}{2\pi r\sqrt{\varepsilon_{eff}}} \qquad (1)$$



For the design of the microstrip and stripline, the per unit length (pul) loss in dB/mm can be estimated using the equation below;

$$Loss\ dB\ (pul) = -4.34\left[\frac{R}{Z_0} + GZ_0\right] \qquad (2)$$

Equation 2 shows a correlation between the impedance and the loss per unit length of the transmission line interconnect structure, where Zo represents the impedance of the structure, R is the pul resistance of the conductor, and G is the pul conductance. For low loss materials were G<<<R, there is a direct correlation between Zo and the insertion loss.

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{Wm}{H} + 1.393 + \frac{2}{3}ln\left(\frac{Wm}{H} + 1.444\right)\right]} \qquad (3)$$

For a microstrip with a dielectric material of thickness H between the ground plane and signal line. By fixing the dielectric thickness in equation (3) the microstrip line width Wm can be modified to vary the impedance.

The impedance of the stripline design can be calculated using:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_R}} ln\left[\frac{1.9(2H+T)}{0.8Ws+T}\right] \qquad (4)$$

where ε_R is the relative permittivity of the dielectric material used. As shown in equation (4), the variation of the stripline width(Ws) can be used to vary the impedance. The interconnect parameters estimated are shown in Table 1.

Table 1. CHANNEL PARAMETERS

	Parameter	Dimensions
Microstrip width	W_m	100, 80 and 45um
Microstrip length	L_m	1, 2, and 5mm
Stripline width	W_s	53 and 25um
Stripline Length	L_s	1, 2 and 5 mm
Crosstalk Spacing	S	25um, 50um and 75um

INTERPOSER STACKUP & MEASUREMENT DETAILS

As 60 mm x 52 mm coreless organic interposer test vehicle was designed using four metal layers, where the top metal layer (M1) contains the microstrip line, M2 and M4 are the ground planes for the stripline connections and M3 contains the striplines. Figure 6 provides the details.

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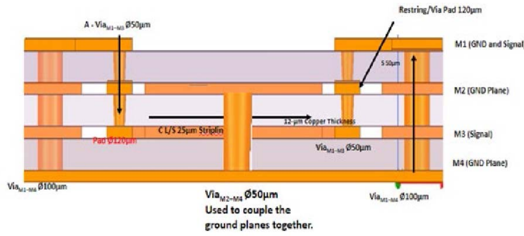

Figure 6. Interposer stackup.

To define the test vehicle stack-up several 3D simulations were performed for communication between the PIC-ACC, with details provided in Table 2. The channel details in Table II were simulated in Ansys HFSS using 50Ω reference impedance. The multi-channel S-Parameters including crosstalk were cascaded and simulated using a 25Gbps data rate. Tachyon material used has advantages as it is a thinner dielectric which translates into increased electrical performance. The structures were constructed by matching to a 200 µm pitch GSG probe or a 250 µm GSSG probe with a two/four-port calibration to the probe tip as the reference plane. The minimum copper thickness used was 5 µm. The probes for the GSG were calibrated using Through-Line-Reflect (TRL) multiline calibration for measurements between 3-100 GHz. The test vehicles were fabricated with a minimum of 25 µm feature dimensions.

Table 2. TEST VEHICLE INFORMATION

Core	N/A
L/S/T (um)	25/25/10
Dielectric (um)	50 (Isola Tachyon 100G)
Via/Pad (um)	60/100
C4 Pitch/Size (um)	100/50
Min Spacing between Chips (um)	600
Layers	4+
Interposer Size (mm)	Large
BGA Pitch/Size	~
Process	Lamination/Subtractive

Two different measurement setups were used to cover the frequency range from 0 to 67 GHz. The measurement from 70 to 100 GHz samples was done using an Anritsu VNA (ME7808) and frequency extenders 3742A-EW. Cascade ACP-110-GSG-200 probes were used to probe these samples. For (70–100 GHz), Agilent E8361C vector network analyzer, mmWave controller, and frequency extenders (V06VNA2) were used. Infinity probes 170-S-GSG-75-BT were used to probe these samples. Line-Reflect-Reflect-Match (LRRM) calibration was performed using the WinCal software. LRRM calibration was used to remove the losses from cables, test heads, and probes. The crosstalk measurements were made using Keysight N5247B PNA-X and ACP65-D-GSSG-250 probes using the SOLT calibration on the VNA.

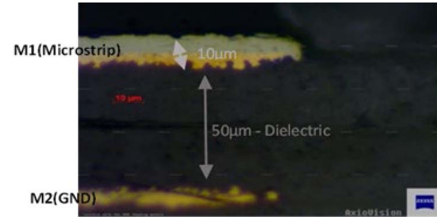

Figure 7. Cross-section image of the two metal layers of microstrip.

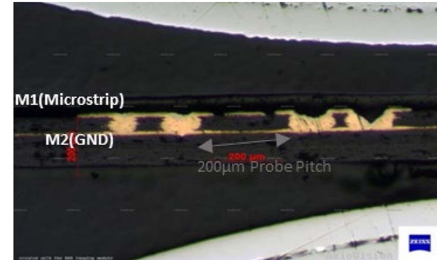

Figure 8. Cross-section image of probe pads of MRR.

The substrates were cross-sectioned and some of the results are shown in Figure 7 and Figure 8. The copper thickness of M1 is seen to be about 10 µm including Ni/Au surface finishes in Figure 7 which is within the desired thickness. Figure 7 shows the dielectric thickness as 50 µm as desired. In Figure 8, the vias inserted under the pads for the Copper-Backed Coplanar Waveguide have a hollow fill creating a non-planarized surface which creates challenges in probing. The fabricated coupon and structures are shown in Figure 9.

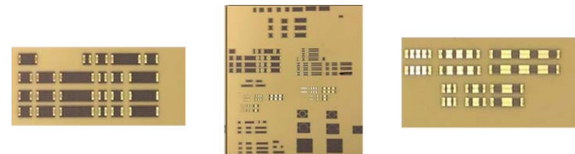

Figure 9. Test Vehicle showing fabricated interconnect structures.

III. MEASUREMENTS

A. Material characterization

The effective dielectric constant was extracted using eq. (1), and the accuracy of the dispersion depends on the accuracy of the measurement at each frequency point and the total circumference. While designing the microstrip ring resonators for 28-56 Gbps designs, the homogeneous isotropic material assumption is an important factor to consider in a model to measurement correlation. Without accurate dielectric material models, it is difficult to close the loop between electromagnetic modeling and actual operation. The high-speed digital performance of the laminate & resulting PCB depends on the quality of the resin, the copper foil, the weave of the glass, and their location when the signal passes over them[7]. Skin effect is also another loss to be considered as it reduces the effective cross-sectional area and increases the resistance. We did not consider conductor roughness in our models which can alter the extracted dielectric constant. Multiple samples were fabricated to allow for statistical variations, and the measurements from coupon to coupon were consistent leading to reliable measurements. During the measurements, there was some difficulty in probing the ground

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pads due to the presence of a via obstruction, which created additional resonances.

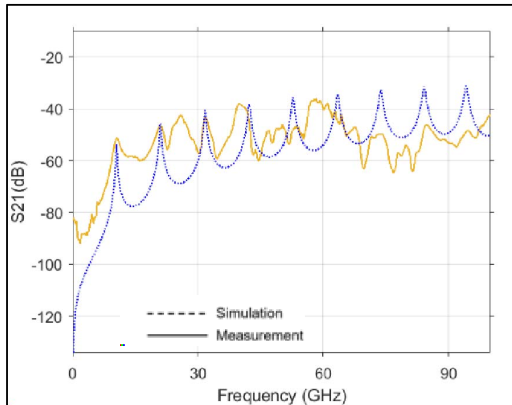

Figure 10. S21 after TRL calibration in MRR Measurement.

In Figure 10, the simulation results are shown for the MRR using a fundamental frequency of 11Ghz. In Fig 10, the measurement results are also shown, where some of the peaks are sharper than the others. Over the frequency range where the resonance peaks are sharp, we extracted a dielectric constant of ~3.28 using equation (1).

B. Microstrip Characterization

For microstrip lines, considering short distances, higher impedance lines can be used for improving interconnect density. The insertion losses through Ansys HFSS simulations and measurements through VNA are compared to quantify the transmission losses. After the measurements, TRL calibration is used. Fig 11 shows the average loss was ~0.3db/mm - 0.4db/mm at the upper frequencies.

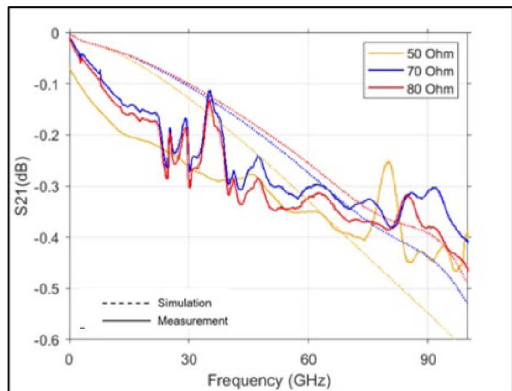

Figure 11. Microstrip dB/mm for 50Ω, 70Ω and 80Ω after de-embedding.

The S21 simulation and measurements are shown in Figure 11 for three impedances for 1mm long lines. The difference between simulation and measurements can be attributed to copper roughness not being considered. Three microstrip line lengths are compared in Figure 12. From the microstrip line measurements it is evident that the longer lines of length 5 mm have a much higher loss, but with a maximum insertion loss of ~2dB at 90GHz.

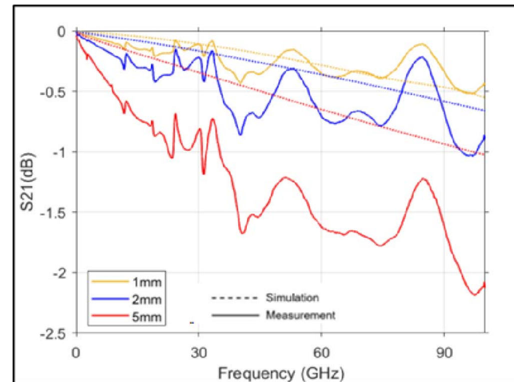

Figure 12. S21(dB) of microstrip line (1, 2, 5mm).

The near-end cross talk (NEXT) measurements are shown in Figure 13 where the maximum cross talk is between 15-20 dB for the three interconnect lengths.

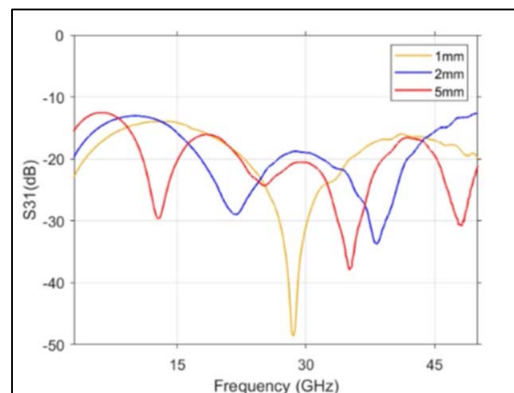

Figure 13. Near End Cross Talk (NEXT) for Microstrip lines.

Since the spacing between the lines can affect the impedance, we also measured structures with different spacings as shown in Figure 14 where the S21 measurements are shown.

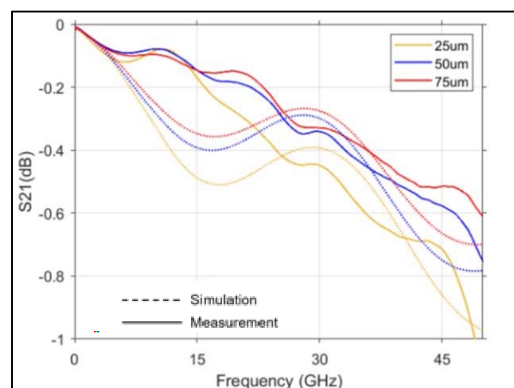

Figure 14. Coupled Microstrip(1mm) at 25um, 50um and 75um spacing.

C. Stripline Characterization

Striplines have a higher loss in general compared to microstrip lines due to the dual ground plane. As noted earlier, vias in the structure introduced resonances. Also, for striplines, a lack of

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sufficient ground vias between the planes on either side of the dielectric can lead to resonances, which were observed in the measurements. Here coupled striplines are investigated. Figure 15 shows the S21 measurements for the striplines for three lengths namely, 1mm, 2mm, and 5mm. Further investigation is necessary for understanding the reduced correlation between the simulation and measurements in the figure.

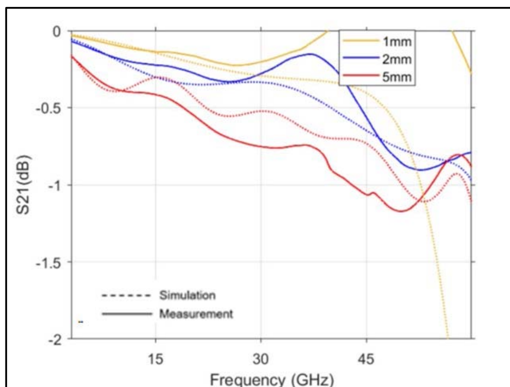

Figure 15. Dembedded coupled Stripline S21(dB) for 1, 2 and 5mm.

The measured near-end cross talk (NEXT) for striplines is shown in Figure 16 in the frequency range up to 50 GHz. As expected, the cross talk is lower than the Microstrip NEXT described earlier below 30 GHz due to the presence of multiple ground planes.

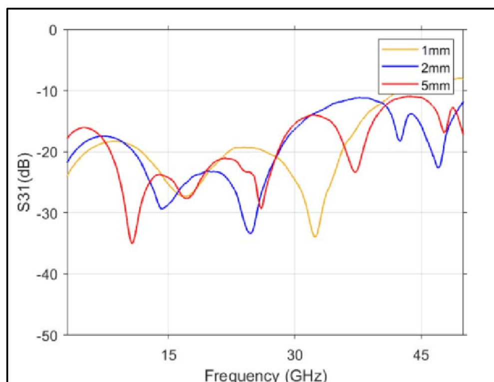

Figure 16. Stripline Near End Cross Talk S31(dB) for 1, 2, 5mm

The estimated loss of stripline ~0.5dB/mm over the frequency range measured. The excess spikes in the stripline measurements can be attributed to the vias needed to connect to the ground planes on either side of the dielectric, where the placement and size of the vias affect the resonances which needs further optimization.

D. Via Characterization

It is important to account for degradation due to vias. In this section, we attempt to characterize one and two-layer copper-filled blind vias. We accounted for the 25um annular pads and 25um drill spacing for the vias as part of the design process. Here the advantage of having a thinner dielectric means with a minimum aspect ratio of 1 we can fabricate smaller vias.

While two different impedances were designed to extract the parasitics of the vias, we focus mainly on one impedance in presenting our results in this paper. Also, during simulations, it was observed that different coplanar lengths when cascaded cause reflections at each transition between the lengths to add up constructively. Hence by using measurement over three different lengths we attempted to capture the complete response of the vias over the entire frequency range. The single-layer via measurements for a daisy chain consisting of four vias is shown in Figure 17 along with the measurements.

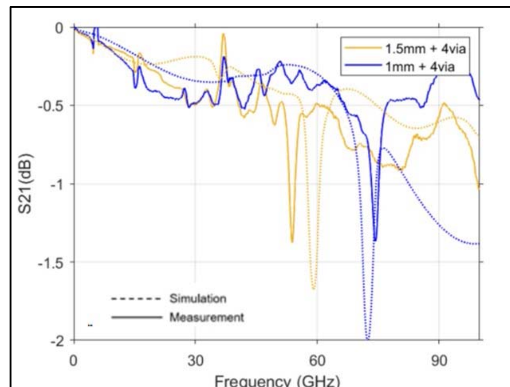

Figure 17. Via measurements and simulation for four vias.

Based on measurements the insertion loss of the vias was extracted as 0.104 dB/via for one layer and 0.134 dB/via for two layers.

E. Microstrip to Stripline Transition

Transitions are necessary to connect the microstrip lines to the striplines through the vias. This transition can create difficulties if not managed well. Here, we show the importance of resonances that can affect the insertion loss significantly.

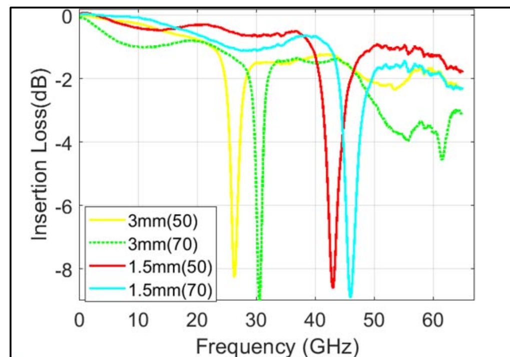

Figure 18. Insertion Loss of via transitions for 50Ω and 70Ω

In Figure 18 we show the S21 measurements for 1.5mm and 3mm long transitions using two impedances (50 and 70 ohms). The impedance of the lines shifts the resonances with the movement of the resonances being sensitive to the transition length.

We simulated these structures for the 3mm long transition and 70 Ohm impedance as shown in Figure 19, which shows good model to hardware correlation.

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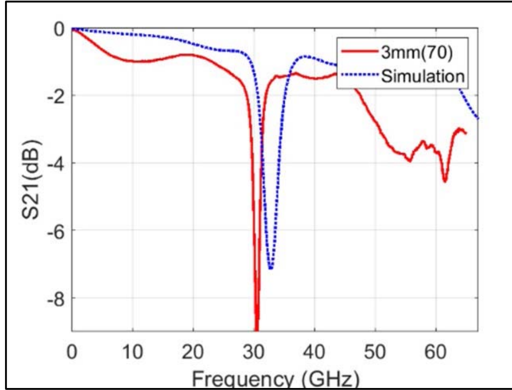

Figure 19. Model to hardware correlation for 3mm long transition.

The cause of these transitions is clearly due to the vias, thereby removing the via parasitics, we were able to improve the S21 results significantly using simulation, as shown in Figure 20.

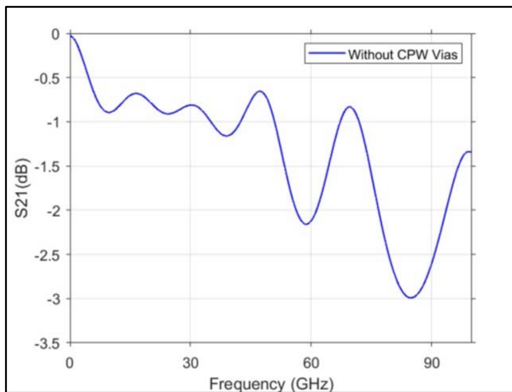

Figure 20. S21 simulation results without vias.

IV. EYE DIAGRAM SIMULATIONS

We used the measurement results to generate eye diagrams of the microstrip line and stripline that include cross-talk. The signals used had a signal swing of 1V, rise/fall time of 20ps, 62.5ps unit interval (UI), with a bit error rate of 10^{-12} using 50-Ohm terminations and ideal drivers. This pseudo-random bit stream (PRBS) corresponds to a bit rate of 16Gbps. The results in Figure 21 show that the eye-opening is quite large for both the microstrip and stripline structures mainly due to the short length of the interconnections, indicating that the organic laminate technology with the high-frequency dielectric material can support such high bit rates.

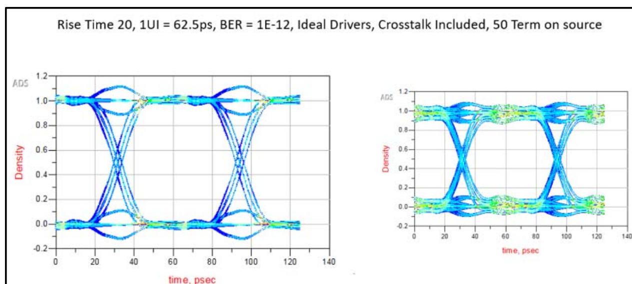

Figure 21. Eye diagrams for Microstrip (left) and Stripline (right).

In the worst-case scenario, we also simulated eye diagrams using a PRBS signal and a 50Ω source termination using the measurement S-Parameters, where the signal frequency coincided with the resonance frequency, as shown in Figure 22. Despite the resonance, we are able to generate an eye-opening large enough for communication.

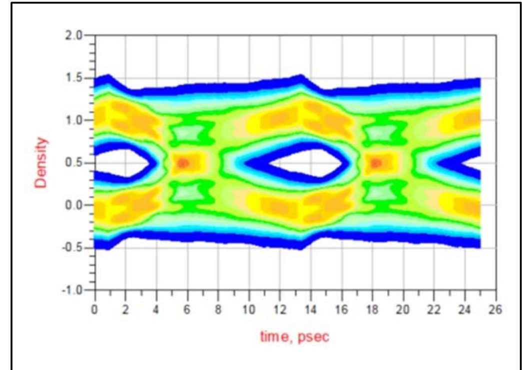

Figure 22. Worst case eye due to resonance.

V. CONCLUSIONS

In this paper, we describe the simulation and measurements results for an organic laminate substrate with a high-frequency dielectric material. To establish communication between the EIC and PIC, we designed different kinds of structures that included microstrip, stripline, daisy chain vias, and transitions, which we measured using a VNA. The S-parameter measurements provided insight on the insertion loss, cross talk, and resonances associated with these structures. Using these measurements, we simulated the eye diagrams and found that despite the anomalies, we were able to support data rates of 16GBps, which was the requirement.

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