Ultra-Efficient Foundry-Fabricated Resonant Modulators with Thermal Undercut

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Abstract: We demonstrate highly efficient vertical junction microdisk modulators with selective substrate undercut in a 300 mm CMOS foundry. The devices achieve record thermo-optic efficiency for sub-5 μm radius, enabling next-generation low-energy, highly-parallel DWDM links.

1. Introduction and Results

Resonant modulators are essential devices for highly energy-efficient dense wavelength-division multiplexed (DWDM) silicon photonic links due to their inherent wavelength selectivity, compact footprint, and low energy consumption [1]. Enabled by silicon's strong thermo-optic coefficient, integrated micro-heaters are typically necessary for such devices to tune and stabilize the resonant wavelength in the face of fabrication (static) and temperature (dynamic) variations. Previous demonstrations have shown modest electro-optic tuning to accommodate temperature variations on the order of 10 K [2, 3], but this range is an order of magnitude below the electronics-induced localized temperature swings possible in co-packaged optical interconnects. Thus, for realistic scenarios, integrated micro-heaters are required to achieve the necessary tuning range. However, such heaters can consume on the order of 25 mW P_π [4], which is prohibitive for low-power applications. Here, we demonstrate an ultra-efficient vertical junction microdisk modulator with an improvement in thermal tuning efficiency greater than 3$\times$ realized through a wafer-scale-compatible selective substrate undercut. Furthermore, the large overlap between the vertical junction and optical whispering gallery mode results in a large modulation efficiency compatible with small CMOS drive voltages. We measure key thermal metrics of $P_\pi = 8.4$ mW and $V_\pi = 2.7$ V for a representative 4.5 μm radius device, achieving record thermo-optic efficiency for a sub-5 μm radius resonant modulator while maintaining a CMOS-compatible voltage. The high efficiency, compact footprint, and wide free spectral range (FSR) of the demonstrated device will enable extreme scaling in the wavelength domain with ultra-low energy consumption for future DWDM silicon photonic links.

The detailed microdisk modulator device design is detailed in ref. [1]. Trench openings were defined in layout around the device (Fig. 1a) to enable the top-side undercut process. The integrated micro-heaters were designed using a doped silicon resistor in the interior of the disk with a 100 nm wide full silicon etch to isolate the heater from the junction contacts. The devices were fabricated on a dedicated 300 mm wafer run through AIM Photonics and designed for full undercut processing at the wafer-scale. While the development fabrication process on test wafers fully released the designed devices (Fig. 1a), the devices from the first full-build wafer were not fully undercut and thus required additional post-processing to complete the isotropic substrate etch (inductively coupled plasma reactive ion etch to remove the $\approx$ 100 nm of remaining buried oxide and vapor phase xenon difluoride etch to selectively remove the silicon substrate [5]). Wafers using an updated undercut recipe are currently under fabrication and are expected to have fully released devices without any post-processing. The fully released devices were then optically characterized with a v-groove fiber array and electrical multi-contact wedge probes to measure the thermal and modulation efficiencies. Assuming that a $\frac{\pi}{2}$ phase shift is possible from temperature swings (Fig. 1c) and an additional $\frac{\pi}{2}$ phase shift is possible from fabrication variations, worst-case tuning of π is required for devices under realistic scenarios. We measure the modulation efficiency to be approximately 60 pm/V, which is on the same order as previous state-of-the-art demonstrations [2, 3]. However, the integrated micro-heater in our device enables a much larger tuning range ($> \pi$) than these previous demonstrations ($< \frac{\pi}{16}$) and only consumes 0.67 mW/nm, yielding a worst-case per-device energy consumption of 8.4 mW. From simulations, we anticipate that this value can be further reduced in next-generation designs to yield $P_\pi \approx 3$ mW (10$\times$ improvement) through optimization of the heater geometry.