Frontiers in Optics + Laser Science (FiO/LS) @ Optica Publishing Group 2022

Learning Bit-Gates With A Resonant Photonic Linear Neuron

Matthew van Niekerk[1,†], Anthony Rizzo[2], Hector Rubio Rivera[1], Gerald Leake[3], Daniel Coleman[3], Christopher Tison[4], Michael Fanto[4], Keren Bergman[2], and Stefan Preble[1]

[1] *Microsystems Engineering, Rochester Institute of Technology, Rochester, NY, USA,*
[2] *Department of Electrical Engineering, Columbia University, New York, NY, USA,*
[3] *State University of New York Polytechnic Institute, Albany, NY, USA,*
[4] *Information Directorate, Air Force Research Laboratory, Rome, NY, USA*

[†] *mv7146@rit.edu*

Abstract: We present a new architecture for performing learning-based tasks directly on an integrated photonic chip. We experimentally realize logical 2-bit gates AND, OR, and XOR to accuracies of 96.8%, 99%, and 98.5%, respectively.

1. Introduction

Neuromorphic photonics has blossomed into a rich field of research and engineering as researchers continue to seek improved methods for efficient computing. The notably attractive attribute of this field is light's linear behavior, which is well-suited to neural network algorithms. Specifically, either with simple beam splitters and phase shifters (wavelength coherent designs) or ring-resonators and photodetectors (wavelength incoherent designs), an integrated photonic circuit can implement any arbitrary vector-vector, or vector-matrix multiplication [1–3]. Wavelength coherent designs fall prey to poor scaling laws, both in physical size and individual optical element count [1, 2]. Wavelength incoherent designs, on the other hand, rely on destroying the signal through detection in order to impart the activation step [3].

Here, we demonstrate a new architecture, which leverages the interference of the coherent design outlined in Ref. [1] and the wavelength parallelism of resonant modulators to dramatically reduce the footprint of a network's linear stage. We use this architecture to demonstrate the learned classification task of recognizing the 2-bit logic gates directly on chip.

2. Circuit Design

The coherent optical linear neuron (COLN) presented in Ref [1] utilizes Mach-Zehnder modulators (MZMs) arranged in a nested branch configuration. The signal is passed to a fan-out, wherein each branch feeds to an input MZM (x_i), a phase shifter ($\pm$), and a weight MZM (w_i); finally all the branches are combined at the fan-in – which plays the role of *coherently* summing the N signals. This circuit maintains a mathematical equivalence to the linear stage of a neural network, where the circuit results in the equation

$$\text{Linear Stage} = \sum_{i}^{N} x_i w_i. \tag{1}$$

For a silicon photonic application platform, we recognize that MZMs are generally large (~ 1 mm^2) on-chip elements. In order to decrease the footprint, we employ microresonator modulators (MRMs) in place of MZMs, since MRMs have an on-chip size of $\sim 10^{-4}$ mm^2. In addition, MRMs enable the same physical circuit to perform *coherent* operation at multiple channel frequencies – effectively creating wavelength diversity for operation, such that we have the result of Eq. 1 *for each wavelength*. We call this architecture concept a wavelength diverse integrated photonic linear neuron (WDIPLN).

3. On-Chip Recognition of Logic Gates

We designed a simple, single wavelength WDIPLN circuit for a first principle demonstration. In Fig. 1 (a), we show a full schematic of the designed photonic integrated circuit (PIC) and experimental setup. The PIC contains two input MRMs – X_1, X_2 – and two weight MRMs – W_1, W_2. We place a bias path in order to validate the full range of $[-1, 1]$ for the weights; however, this path is not part of the trained network. We define a simple neural network design with two inputs, one hidden layer with two nodes, and a single output node, as seen in Fig. 1 (b).

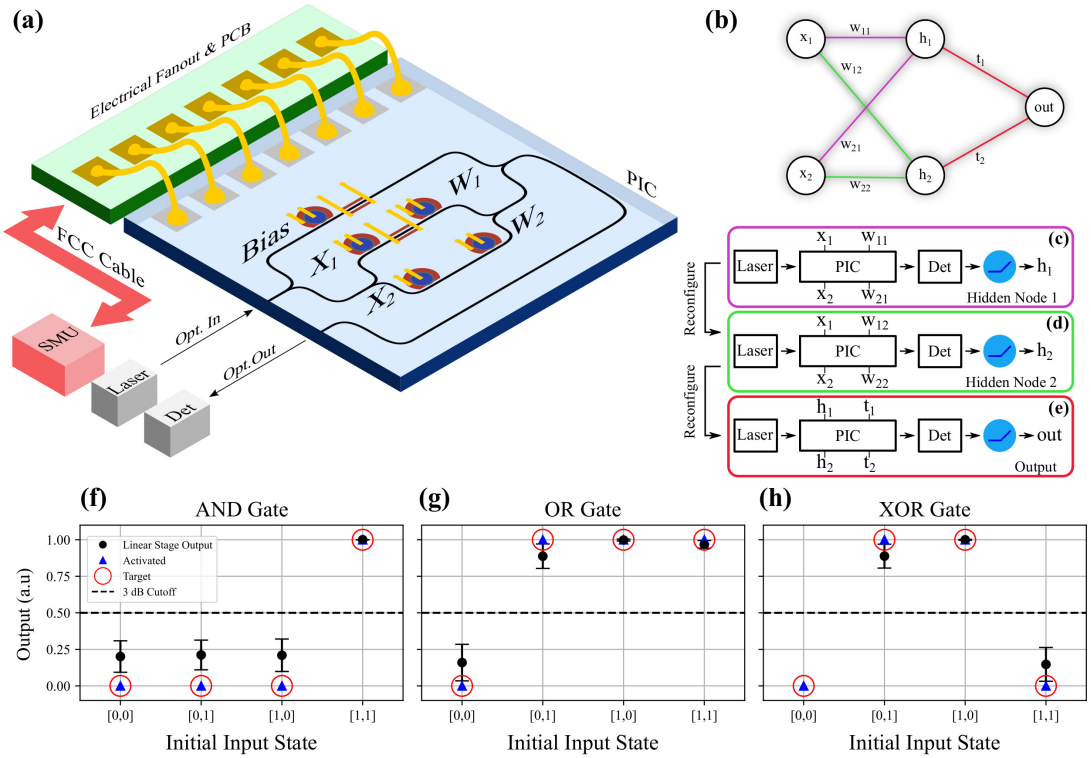

Fig. 1. (a) The PIC schematic and experimental set up. (b) The neural network architecture for training and implementing the 2-bit logic gates. (c)-(e) The reconfiguration scheme for updating and recycling the PIC in (a) for the full network. (f)-(h) The results of 2-bit gates as measured through the PIC.

We trained the neural network offline, determined the appropriate weight parameters $(w_{11}, w_{12}, w_{21}, w_{22}, t_1, t_2)$, and stored these values. We characterized the transfer function of a single MRM and used this to impart a given weight by assuming all the rings in this circuit were identical. We represent a "1" and "0" on-chip by tuning the MRM to off-resonance or on-resonance, respectively. With these building blocks, we use the method outlined in Fig. 1 (c-e) to implement the simple neural network by reconfiguring the circuit three times to capture the behavior of the network. A future design would bypass reconfiguration by integrating multiple circuits on a single PIC.

The selected 2-bit logic gates are AND, which gives a response of "1" only when both inputs are also "1," OR, which gives a response of "1" when any of the inputs are 1, and XOR, which gives a response of "1" when only one of the inputs are "1." Using the method in Fig. 1 (c-e), we implemented the three logic gates iteratively and with no thermal corrections for resonant drift, at a single evaluation wavelength of $\lambda = 1{,}526$ nm. The results are presented in Fig. 1 (f-h), with each the AND, OR and XOR gates achieving accuracies of $96.8\%, 99\%$, and 98.5%, respectively.

References

1. G. Mourgias-Alexandris *et al.*, "Neuromorphic photonics with coherent linear neurons using dual-iq modulation cells," *Journal of Lightwave Technology*, 2019.
2. Y. Shen *et al.*, "Deep learning with coherent nanophotonic circuits," *Nature Photonics*, 2017.
3. A. N. Tait *et al.*, "Broadcast and weight: an integrated network for scalable photonic spike processing," *Journal of Lightwave Technology*, 2014.

Acknowledgements: This work was supported by Air Force Research Laboratory (FA8750-21-2-0004 and FA8650-21-2-1000). The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the United States Air force, the Air Force Research Laboratory or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. M.v.N funded by NSF award DMR-1747426.