Silicon Photonics Chip I/O for Ultra High-Bandwidth and Energy-Efficient Die-to-Die Connectivity

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Abstract—Embedded silicon photonics (SiPh) is promising to enable ultra-high bandwidth system-wide connectivity with vastly reduced energy consumption by integrating optics deeply within computing sockets. We present the design and characterization of a dense wavelength-division multiplexing (DWDM) SiPh transceiver chip, featuring a unique architecture in the multi-FSR regime and targeting a shoreline bandwidth density of 2 Tbps/mm with a sub-pJ/b energy consumption, providing a viable path toward die-to-die connectivity at scale.

1. Introduction

Traffic demands in data centers and high-performance computing systems have grown exponentially over the past decade, driven by the proliferation of data-intensive workloads in machine learning, big data analytics, and especially deep learning (DL)–based artificial intelligence (AI) applications. The recent demonstrations of huge potentials of large language models in natural language processing and content generation have further accelerated the technological progress toward data ubiquity with the adoption of increasingly larger DL models and datasets [1]. The ongoing trend has sparked tremendous effort improving the capabilities of the computational hardware, notably through aggressive parallelism and specialization [2,3], far outpacing the progress of the underlying communication infrastructure [4]. As a result, moving massive data off and between chips has become the bottleneck of the computing performance and energy efficiency, gating the continuous scaling of such systems toward exascale [5].

Optical interconnects have been widely recognized as a viable solution to providing uniformly high-bandwidth data communication across a wide range of distances, leveraging the low-loss and multiplexing nature of light in fiber optics [6]. However, the gain from replacing electrical links with optical ones starts to plateau at shorter distances, predominantly bottlenecked by the energy consumption associated with the electrical-optical (EO) conversion at chip edges [7]. Existing solutions based on pluggable optics require electrical signals to travel along centimeter-long copper wires before reaching the EO interface. Such a form factor significantly limits the achievable data rate per interface without incurring substantial energy cost, prohibiting further upscaling of the system connectivity [8]. To this end, embedded silicon photonics (SiPh) optical interconnects have emerged as a promising avenue for bringing the optics closer to the computing sockets [9–12], effectively eliminating the distance dependency of the bandwidth density–energy efficiency product for data links across multiple network hierarchies [13]. In particular, SiPh microresonator-based modulators and filters [14,15] demonstrate excellent wavelength selectivity with compact footprints that—when combined with recent advances in optical frequency comb sources [16–18]—provide an elegant solution to realizing dense wavelength-division multiplexing (DWDM) links [19,20] without relying on bulky distributed feedback (DFB) laser arrays or dedicated (de-)multiplexers.

Silicon nitride (Si_3N_4) Kerr combs operating in the normal group velocity dispersion (GVD) regime are of growing interest to DWDM applications, thanks to their capability of generating hundreds of evenly-spaced low-noise frequency channels from a single continuous-wave (CW) laser source, with better conversion efficiency, power per line, and spectral flatness compared to alternative technologies [21]. The massive parallel frequency channels open up the possibility of achieving petabit-scale package escape bandwidth at sub-pJ/b energy consumption [13], while also posing challenges in terms of how physical limitations of resonant devices can be circumvented by architectural innovations to support such scaling. Specifically, due to the periodic nature of the resonator resonances in the frequency domain, the traditional link architecture for microresonator-based DWDM—typically featuring a single bus of cascaded microresonators [22–25]—requires all communication channels to be placed within a single free spectral range (FSR) of the resonator. The maximum optical bandwidth supported by this architecture, hereafter referred to as the *single-FSR* regime, is thus upper bounded by the resonator's FSR, which, in turn, is physically limited by the minimum resonator radius [26] and only a fraction of the spectral bandwidth of state-of-the-art frequency comb implementations [21]. To address this challenge, the authors have recently proposed a scalable link architecture in the *multi-FSR* regime [20,27,28] that allows for resonator FSRs smaller than the total optical bandwidth of the link while still being able to communicate over all channels with minimal crosstalk penalties, unlocking the design space for ultra-broadband Kerr comb–driven DWDM links.

In this study, we present our latest design and characterization of a SiPh microresonator-based DWDM transceiver (TRx) chip in the multi-FSR regime, featuring 64 channels per fiber output at 100 GHz channel spacing and targeting a chip shoreline bandwidth density of over 2 Tbps/mm with a sub-pJ/b energy consumption. In Section 2, we briefly review the link architecture and the photonic integrated circuit (PIC) design with considerations for electronic co-packageability. In Section 3, we present the design and characterization of key PIC enabling devices and components, including even-odd (de)-interleavers with automatic tuning, ultra-efficient vertical-junction microdisk modulators, and add-drop filter arrays. In Section 4, we discuss the energy implications of fabrication process variations and foundry-compatible substrate undercuts based on wafer-scale measurement data. In Section 5, we conclude the paper with a summary of the work and future outlook.

2. Link Architecture and Chip Design

Traditional microresonator-based DWDM link architectures in the single-FSR regime face fundamental challenges when the total optical bandwidth of the comb source scales beyond the resonator FSR. Specifically, since a microresonator exhibits periodic resonances at integer multiples of its FSR, there exist unwanted resonances other than the design target, a.k.a., *resonance aliases*, that could potentially overlap with non-target comb lines and result in severe crosstalk. Meanwhile, packing more channels into a single FSR risks introducing excessive inter-modulation crosstalk due to reduced channel spacing, with past experiments showing < 100 GHz channel spacing impractical [29]. While it is possible to have microresonators with larger FSRs by adopting smaller radii [30–32], it is an unsustainable solution to massive wavelength scaling due to physical limitations on the minimum microresonator size and accompanying design/manufacturing complexities regarding integrated heaters, radio frequency (RF) contacts, as well as electrical parasitic and process variation containment. Another approach, a.k.a., *band-interleaving*, tackles the problem by subdividing the incoming comb channels into multiple narrower bands, each fitting into a resonator FSR [33]. However, this approach incurs stringent requirements on the performance of the (de-)interleaving devices, such as sharp pass-band roll-off, broadband crosstalk suppression, as well as decent tunability, and thus relies on the maturity of design and fabrication of novel devices such as on-chip dichroic filters [34,35] and contra-directional couplers [36,37]. In this study, we base our transceiver PIC design on the multi-FSR regime enabled by an *even-odd interleaving* scheme, as previously described in [27]. This section briefly reviews the link architecture and the PIC design.

2.1. Scalable Link Architecture

As described in [27] and shown in Fig. 1a, the TRx link is designed to be driven by a Si_3N_4 dual-ring normal GVD Kerr comb that generates up to hundreds of low-noise frequency channels with 100 GHz channel spacing centered at 1505 nm (S-Band). At the transmitter (Tx) side, the incoming comb lines are subdivided by two stages of de-interleavers—the FSRs of which designed to be 200 GHz and 400 GHz, respectively—onto four buses before traversing

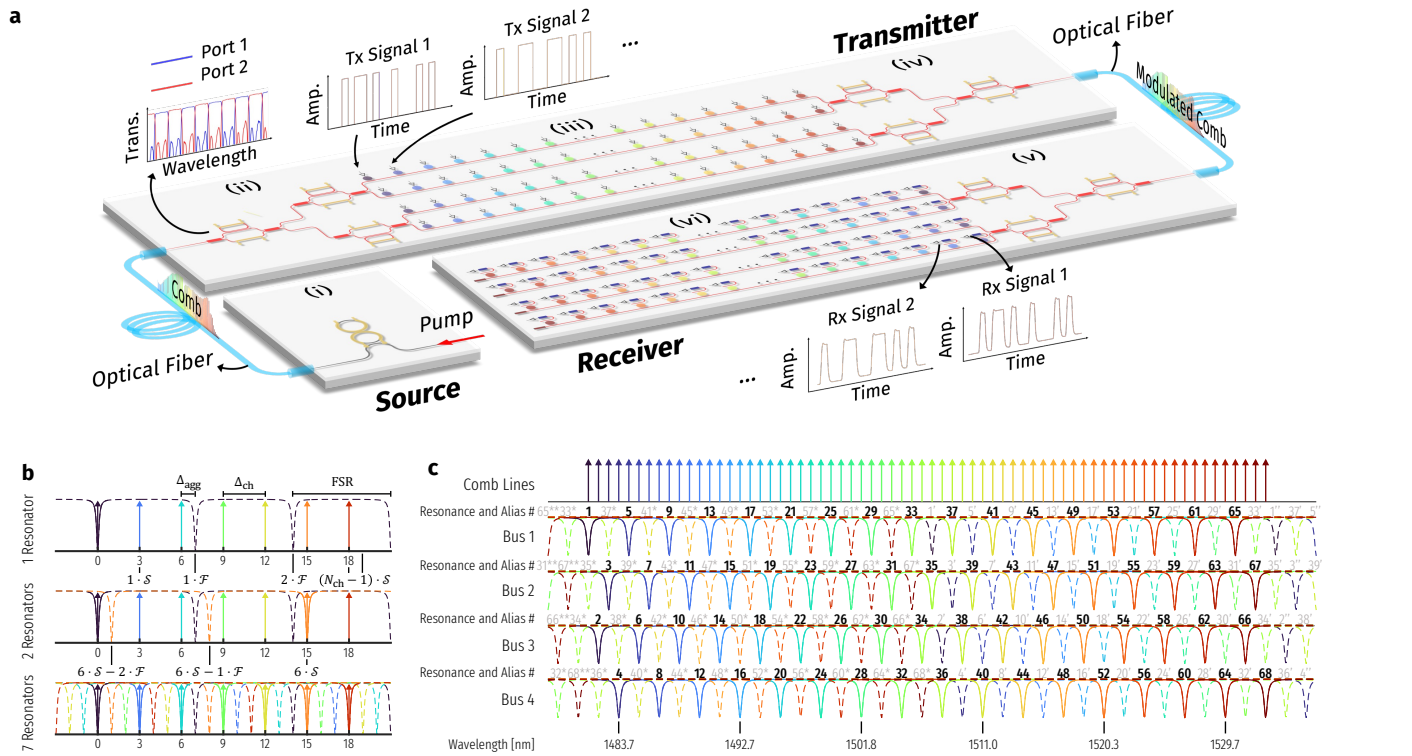

Figure 1. (a) Scalable link architecture based on even-odd interleaving. The end-to-end link consists of (i) a normal GVD Kerr comb, (ii) Tx de-interleavers, (iii) microresonator modulators, (iv) Tx interleavers, (v) Rx de-interleavers, and (vi) microresonator filters and photodetectors. **(b)** An exemplar multi-FSR arrangement for $(\mathcal{S},\mathcal{F})=(3,7)$ [Eqs. (1a) and (1b)] showing the placement of resonance aliases (dashed) between communication channels (solid) ensured by the co-prime rule [13]. **(c)** The multi-FSR arrangement adopted for the transceiver link in this study, with $(\mathcal{S},\mathcal{F})=(2,17)$, allowing up to 17 channels per bus achievable by microresonators with a moderate 25.69 nm FSR. Asterisks (primes) denote the aliases to the blue (red) end of the nominal resonance.

separate banks of cascaded microresonator modulators. Each stage of de-interleaver splits the incoming wavelengths into "even" and "odd" groups, effectively doubling the channel spacing while nearly preserving the total optical bandwidth seen on each output port. Each resonant modulator can modulate a distinct wavelength channel while nearly appearing transparent to other channels on the bus. The modulated signals from the four buses are recombined by two stages of even-odd interleavers into a single fiber output. Symmetrically, at the receiver (Rx) side, the modulated signals are de-interleaved and sent to respective banks of cascaded microresonator filters that drop each channel onto a photodetector (PD) for sensing.

Since the comb lines on each bus span an optical bandwidth of over 50 nm, it is challenging, if not infeasible, to design microresonator modulators with integrated electronic contacts for an even larger FSR due to a prohibitively small physical dimension that raises manufacturability concerns [38]. As a result, the resonator FSR must be carefully chosen to prevent resonance aliases from overlapping with non-target comb lines in the multi-FSR regime. We have mathematically formulated the multi-FSR design principles in [13], from which a valid multi-FSR channel arrangement can be elegantly derived by picking a pair of co-prime integers $(\mathcal{S},\mathcal{F})$ satisfying

$$\begin{cases} \mathcal{S}=\dfrac{\Delta_{ch}}{\Delta_{agg}}, & \text{(1a)} \\ \mathcal{F}=\dfrac{\mathrm{FSR}}{\Delta_{agg}}, & \text{(1b)} \end{cases}$$

where Δ_{ch} is the effective channel spacing on each bus after de-interleaving, Δ_{agg} is the reduced spacing between a channel and its nearest aggressor alias, and FSR is the resonator free spectral range. Fig. 1b visualizes how the co-prime rule ensures the resonance aliases to fall between the communication channels with an example for $(\mathcal{S},\mathcal{F})=(3,7)$, meaning that up to 7 resonators can be arranged along a bus with resonance aliases placed at every one third of the channel spacing.

For the TRx architecture in Fig. 1a, which features a total of 64 channels arranged into four buses, we choose $(\mathcal{S},\mathcal{F})=(2,17)$, as illustrated in Fig. 1c, allowing up to 17 channels per bus achievable by microresonators with a moderate 25.69 nm FSR. The optimal selection of $\mathcal{S}$, $\mathcal{F}$, and FSR involves various trade-offs between the aggregated data rate, crosstalk penalties, and link yield, for which a more holistic design space exploration is provided in [28]. With 16 microresonator modulators/filters placed 400 GHz apart on each bus, the transceiver can effectively perform 64-channel DWDM targeting a 1.024 Tbps/fiber bandwidth capacity with a moderate data rate of 16 Gbps/channel.

2.2. Photonic Integrated Circuit Design and Fabrication

We designed a transceiver PIC featuring the abovementioned scalable link architecture in a fabrication process co-developed with AIM Photonics, which includes custom vertical-junction implants with optimized doping conditions and wafer-scale substrate undercuts for improved thermal tuning efficiency [39, 40]. Fig. 2 shows the microscope images of the fabricated PIC. Each PIC consists of four groups of Tx/Rx arrays, each targeting a 4.096 Tbps/group data rate. Each group of Tx/Rx arrays consists of four 1.024 Tbps links with the architecture described in Sec. 2.1 and Fig. 1a. For electronic integrated circuit (EIC) co-packageability, the PIC signal pads are placed at a 55 µm pitch and routed with considerations for minimizing the parasitic resistance and capacitance of the RF traces. Fig. 2b shows the pad arrays of the Tx cells as an example. The PDs after the resonator drop-ports provide electrical feedback for locking the resonance wavelengths to their target comb lines. Notable implementations of feedback control logics have been reported leveraging the drop-port PD signal [41–45]. The PIC pads will be µ-bumped after fabrication for flip-chip bonding with the EIC driver chip designed accordingly, an approach demonstrated feasible in past works [12, 46]. Wafer-scale substrate undercuts are placed near the resonant modulators/filters as well as the (de-)interleavers (Fig. 2c) for improving the thermal tuning efficiency of and reducing the thermal crosstalk between the thermal phase shifters [39, 40, 47]. The edge coupler array is placed at a 127 µm pitch

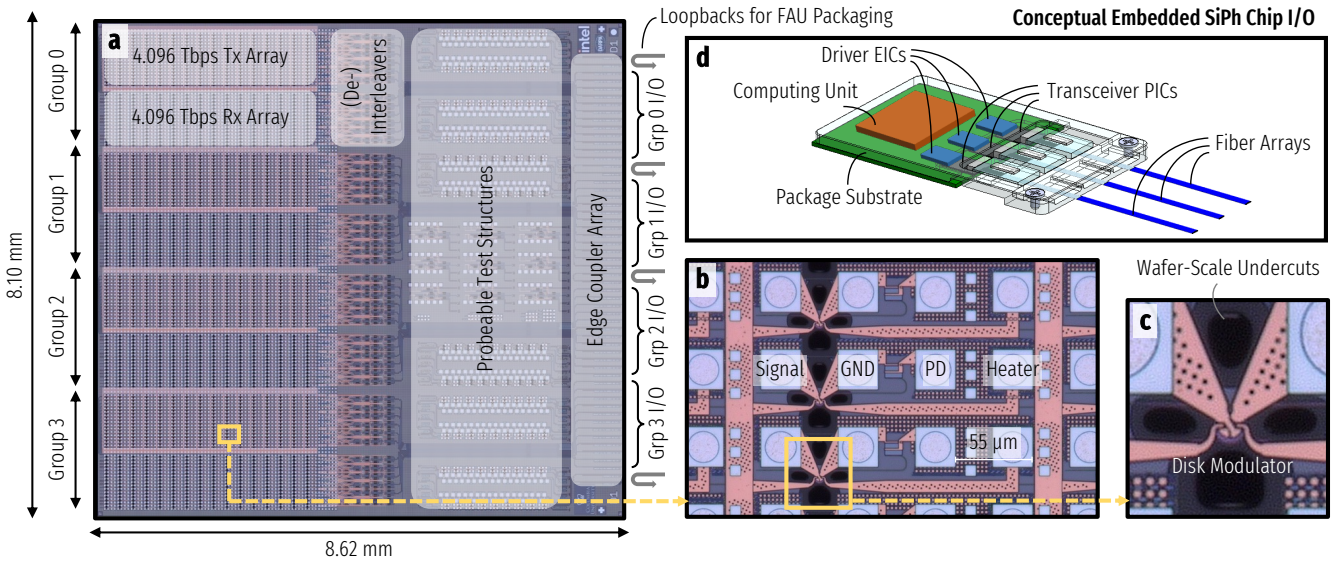

Figure 2. Microscope images of the designed and fabricated transceiver PIC, where each **(a)** 8.10 mm×8.62 mm chip consists of four groups of Tx/Rx arrays targeting 4.096 Tbps/group, probeable test structures of link subcomponents for pre-packaging characterization of process variations and screening of KGDs, and custom suspended edge couplers [12] providing low-loss optical I/O. Each 4.096 Tbps transceiver group consists of four 1.024 Tbps links with the architecture of Fig. 1a. The Tx/Rx arrays feature **(b)** electrical pads at a 55 µm pitch for EIC flip-chip bonding and **(c)** wafer-scale substrate undercuts for improving the thermal tuning efficiency of and reducing the thermal crosstalk between the thermal phase shifters. **(d)** A conceptual chip I/O configuration shows multiple transceiver PICs embedded onto a single platform, next to the computing socket.

along a single side of the PIC for optical input/output (I/O), including four pairs of loopbacks (Fig. 2a) for fiber array unit (FAU) alignment. Custom suspended edge couplers are adopted, which have shown to improve the coupling loss down to –1.1 dB/facet [12], compared to the –3 dB/facet of the standard edge couplers from the process design kit. Between the edge couplers and the (de-)interleavers is a keep-out zone (KOZ) reserved for packaging. However, grating-coupled probeable test structures of the link subcomponents are placed in the KOZ (Fig. 2a) and can be accessed before packaging for identifying known good dies (KGDs) and providing qualitative insights on link performance and yield. Finally, a 16.384 Tbps aggregated bandwidth is able to escape from a single 8.10 mm side of the PIC, resulting in a shoreline bandwidth density of 2.023 Tbps/mm at 1.024 Tbps/fiber. In Fig. 2d, a conceptual configuration for embedded SiPh chip I/O is shown, where multiple transceiver PICs can be co-packaged with the computing unit on a single platform, bringing high-bandwidth optical connectivity closer to the computing socket.

3. Component Design and Validation

The design of the transceiver PIC involves the tight integration of multiple constituent components, notably even-odd (de-)interleavers and microresonator-based modulators and filters. In this section, we present component-level design and validation of the key building blocks of the transceiver PIC.

3.1. Compact Even-Odd (De-)Interleavers

As described in Sec. 2.1 and illustrated in Fig. 1a, even-odd (de-)interleavers are required to expand the effective channel spacing to accommodate the resonance aliases present in the multi-FSR channel arrangement of the cascaded resonator arrays. While basic Mach–Zehnder interferometer (MZI)–based interleavers are compact and relatively straightforward to design, they are prone to fabrication/environmental perturbations and have a limited channel capacity due to the group velocity dispersion of silicon-on-insulator waveguides. In our link design, we adopt a modification of the MZI, known as a ring-assisted MZI (RAMZI), for the required even-odd (de-)interleaving operation. RAMZIs incorporate ring resonators to achieve flat-top pass-bands [48, 49], making it more resilient to both perturbations and the FSR mismatch w.r.t. the comb source, while having a more compact footprint than alternative structures, such as cascaded MZIs [50, 51], that achieve a similar flat-top response.

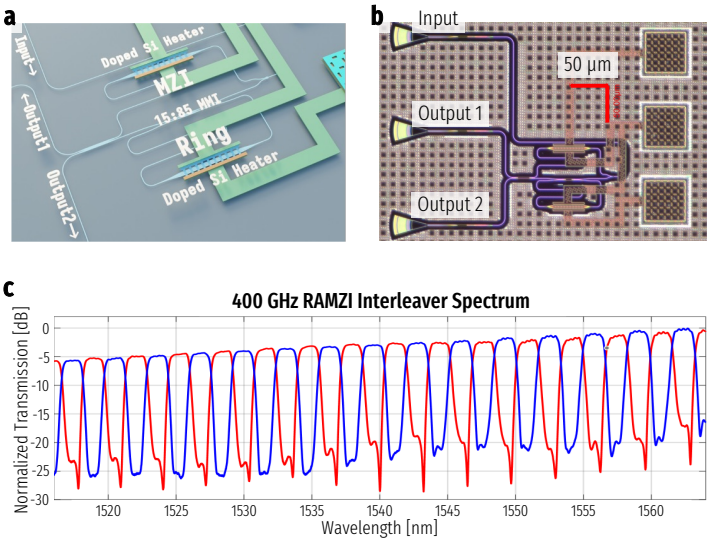

Figure 3. (a) Design rendering of an RAMZI with a 400 GHz FSR. **(b)** Microscope image of the fabricated device. **(c)** Measured transmission spectra of the interleaver. The red and blue curves correspond to the two output ports.

3.1.1. Device Design and Characterization

The RAMZIs are designed with an FSR twice of the channel spacing of the incoming signals to achieve even-odd (de-)interleaving. In the case of this study, the first stage and the second stage (de-)interleavers (Fig. 1a) are designed for 200 GHz and 400 GHz FSRs, respectively. To achieve a broadband flat-top response, a compact multi-mode interferometer–based coupler with 15:85 splitting ratio is implemented for effective coupling into the ring. The effective path length of the ring needs to be approximately twice the MZI arm length difference. Fig. 3a shows a schematic rendering of a 400 GHz RAMZI as an example, and Fig. 3b is the microscope image of the fabricated device. The measured transmission spectra, as shown in Fig. 3c, exhibit a flat-top response after applying 1 V to the phase shifter on the MZI arm, with an extinction ratio of $>$ 20 dB over 50 nm bandwidth for both output ports. It should be noted that the unevenness in the envelope of the spectrum

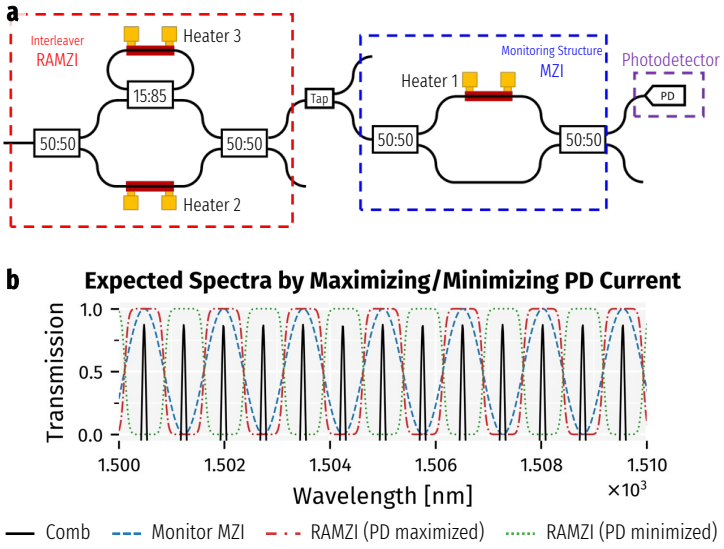

Figure 4. (a) Schematic of the RAMZI interleaver with an auxiliary monitoring structure. **(b)** Simulated RAMZI and monitor MZI spectra when the PD reading is maximized/minimized.

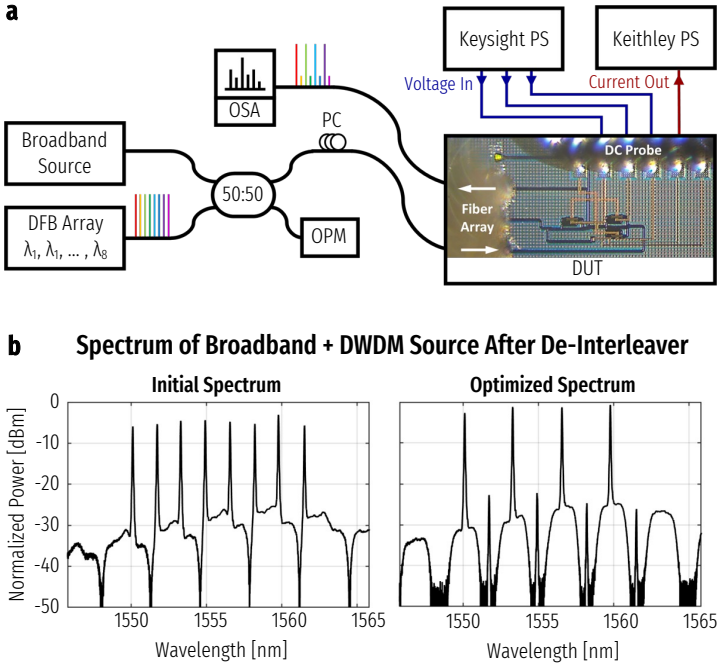

Figure 5. (a) Experimental setup for the interleaver auto-tuning process, where PC: polarization controller, OPM: optical power meter, PS: power supply, and DUT: device under test. **(b)** RAMZI interleaver spectra with DWDM source before and after the auto-tuning, showing an optimized extinction ratio of over 20 dB and the precise alignment of the pass-bands to the DWDM channels after tuning [55].

is primarily introduced by the grating coupler used in the test structure, rather than the interleaver itself. The custom edge couplers used in the transceiver PIC design are expected to have a uniformly low insertion loss across the optical band of interest [12].

3.1.2. Automatic Tuning

The (de-)interleavers in the transceiver PIC are also equipped with a monitoring PD for implementing automatic compensation of phase errors—vital to achieving the desired flat-top response—as well as automatic alignment of the pass-/stop-bands with the DWDM channels. Despite that monitored auto-tuning architectures have been demonstrated for various types of optical filtering devices [52–54], directly tapping either one of the RAMZI output ports for photocurrent monitoring would result in a constant readout, as explained in [51], regardless of the voltages applied on the thermal phase shifters. To address this challenge, we introduce an auxiliary monitoring structure composed of an MZI with an identical FSR to that of the RAMZI, followed by a PD, as illustrated in Fig. 4a. The resulting photocurrent as a function of the thermal tuning voltages is no longer a constant. We have verified through equation-based analyses as well as simulations that the PD current reading will reach its maximum when the pass-bands of both the RAMZI and the monitor MZI are aligned with the DWDM channels, and will reach its minimum when their pass-bands offset with one another by a single channel spacing, as illustrated in Fig. 4b.

We experimentally verified the automatic tuning of the interleavers in a test setup outlined in Fig. 5a. The setup consists of eight DFB lasers with a 200 GHz channel spacing, acting as the DWDM source. The DWDM channels are directed into the interleaver through an angled fiber array and grating couplers, combined with a broadband light source. The broadband source is used for visualizing the interleaver spectrum shape under the optical spectrum analyzer (OSA), and its power is controlled to be much smaller than the DWDM source so that it has negligible impact on the auto-tuning process. The output light from the interleaver is examined by a Yokogawa OSA, allowing for real-time spectrum inspection during the optimization process. It should be noted that the broadband source and the OSA serve only for visualization purposes and do not assist the auto-tuning process. For interleaver thermal control, a direct current (DC) probe is landed on the six pads, connecting the interleaver structure to the DC power supplies. A Keysight multi-channel power supply delivers voltages to the three heaters, acting as the optimization inputs, while a Keithley high-precision power supply provides bias voltage to the PD, reading the generated photocurrent as the optimization target. The adjustment to the heater power at each step is performed in a binary search manner as described in [51]. Fig. 5b shows the interleaver transmission spectra before and after the automatic tuning process, demonstrating an optimized extinction ratio of over 20 dB and the precise alignment of the pass-bands to the DWDM channels after tuning. More details on the interleaver device design, tuning algorithm, and evaluations are provided in [55].

3.2. Resonant Modulator Arrays

In order to validate the transmitter functionalities before EIC integration, we designed and fabricated a test link that has the same modulator and edge coupler designs as the PIC. As shown in Fig. 6a, the test link follows the multi-FSR configuration of Fig. 1c, consisting of 68 Tx modulators arranged into 4 buses. Each modulator is designed to match a distinct wavelength of a 100 GHz comb, which is being co-developed with the PIC by our collaborators. Each bus of cascaded modulators is edge coupled from both ends, without traversing (de-)interleaver stages which are independently verified as described above. Each modulator has two RF pads for modulation and two DC pads for thermal tuning of resonance wavelengths. The RF and DC pads are placed two rows apart, as shown in Fig. 6b, to allow for simultaneous landing of the RF and DC probes. Fig. 6c plots the transmission spectrum of a Tx bus as an example, confirming that the resonances aliases fall between the nominal resonances, satisfying multi-FSR requirements. The channel arrangement closely matches the architectural design shown in Fig. 1c. In the following, we present the design and characterization of the custom microresonator modulators.

3.2.1. Custom Vertical-Junction Microdisk Modulators

Integrated resonant modulators allow for wavelength-selective data encoding in an efficient and compact form factor. Microdisk modulators with vertical-junction depletion-mode modulation are particularly attractive for energy-efficient DWDM implementations, as they can be driven by modest CMOS-compatible voltages [26]. The microdisk's whispering gallery mode requires that all electrical contacts be placed within the external radius of the modulator, as there must be a clean full etch at this boundary to ensure that radiative

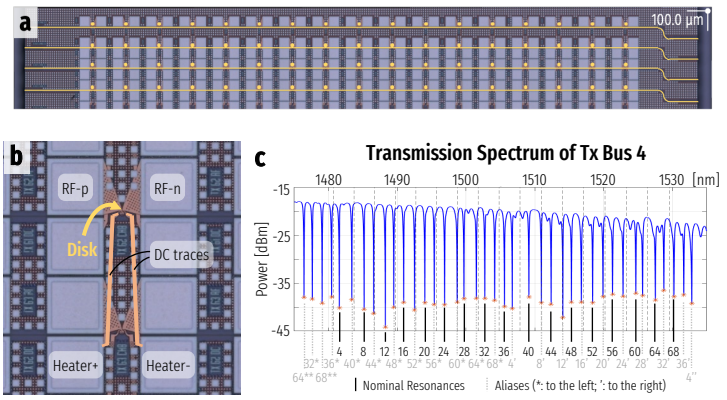

Figure 6. (a) Microscope image of the test link for microresonator modulator arrays, where **(b)** the RF and DC pads are placed two rows apart to allow for simultaneous landing of the RF and DC probes. **(c)** Exemplary transmission spectrum from the 4th Tx bus, matching and validating the multi-FSR architectural design of Fig. 1c.

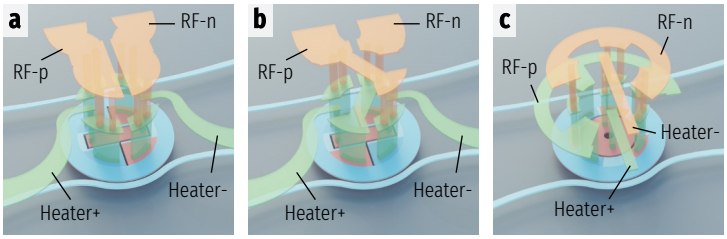

Figure 7. Illustrations of modulator RF contact placement schemes: **(a)** the traditional left-right contacts as seen in [13]; **(b)** the quadrant contacts featured in this transceiver PIC design; and **(c)** the experimental interleaved contacts demonstrated in [56] for incorporation into future chip design. The layer thicknesses are not to scale in order to show the contacts and vias.

bend loss does not degrade the resonator's quality factor (Q) [38]. As the modulator radius decreases, the series resistance—key determinant of the modulator's RC bandwidth—increases, because the foundry design rules regarding minimum metal spacing limit the number of parallel RF contacts. This limit is exacerbated with the inclusion of an integrated heater, which requires room for two additional contacts within an already constrained area [56].

To address this challenge, we developed new contact placement schemes that distribute the RF contacts more evenly across the junctions to reduce the series resistance and improve the modulation bandwidth and efficiency. Compared to the traditional *left-right* scheme (Fig. 7a), where the RF contacts to the P and N junctions are placed onto two distinct halves of the microdisk [13, 31, 57], the transceiver PIC in this study adopts a *quadrant* scheme, as illustrated in Fig. 7b and shown in Fig. 2c, where we divide the doping region into four quadrants and arrange the P/N contacts in a criss-cross pattern. We also took one step further by introducing a new *interleaved* scheme, as illustrated in Fig. 7c and detailed in [56], where the contacts alternate between P and N, analogous to the arrangement of the interleaved lateral-junction ring modulators [58].

Quadrant Contact Modulator Characterization The quadrant contact modulators, featured in the transceiver PIC, are characterized in the test link described in Fig. 6. From the transmission spectra of the modulator buses (an example given in Fig. 6c), we extract the average FSR of the microdisks to be 25.64 nm, closely matching the design target of 25.69 nm. We extract the resonator Q, full width at half maximum (FWHM), and extinction ratio (ER) by fitting a Lorentzian function to each nominal resonance, as seen in Fig. 8a. The average Q, FWHM, and ER are found to be ~7000, 0.22 nm, and 20 dB, respectively. The integrated heater exhibits a 250 Ω resistance (Fig. 8b left), reasonably close to the design target of 200 Ω and expected to be further

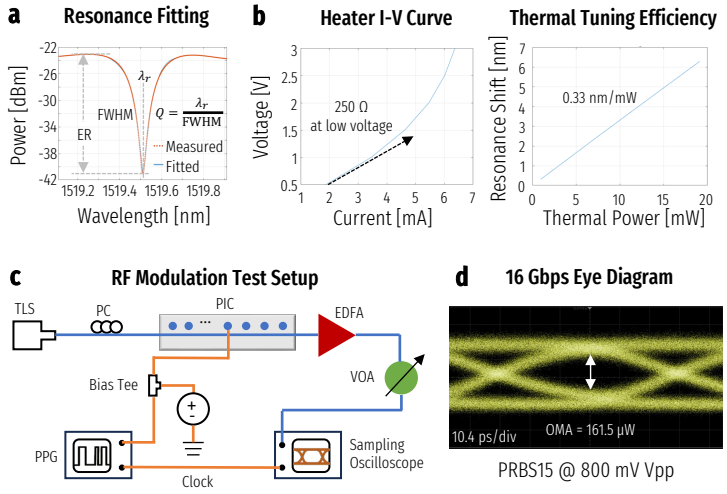

Figure 8. Characterization of the quadrant contact modulator: **(a)** average Q, FWHM, and ER extracted as ~7000, 0.22 nm, and 20 dB, respectively; **(b)** thermal tuning efficiency measured as 0.33 nm/mW, achieved by a 250 Ω integrated heater; **(c)** RF modulation test setup; and **(d)** open eye diagram at 16 Gbps with PRBS15 driven by 800 mV peak-to-peak voltage.

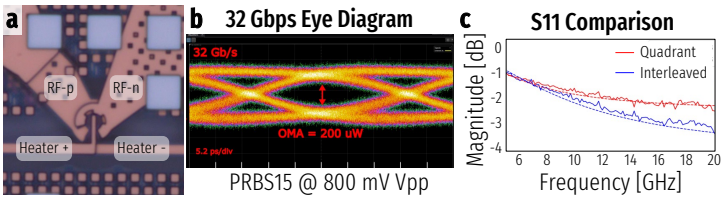

Figure 9. **(a)** Microscope image of a fabricated interleaved contact microdisk modulator. **(b)** Open eye diagram at 32 Gbps with PRBS15 driven by 800 mV peak-to-peak voltage. **(c)** Measured S11 frequency response after de-embedding the pads and connected metal traces, showing reduced back reflections due to better impedance matching with greater number of parallel interleaved contacts [56].

improved in future design. By applying a series of voltages to the heater and observing the shift in the resonance wavelength, a 0.33 nm/mW tuning efficiency is characterized for the modulators (Fig. 8b right).

As shown in Fig. 8c, we characterize the RF performance of the quadrant contact modulators with a non-return-to-zero (NRZ) pseudo random bit sequence (PRBS) that is $(2^{15} - 1)$-bit long, generated by an Anritsu MP1900A pulse pattern generator (PPG). A HyperLabs HL9447 bias tee was used for combining a DC reverse bias of –1.2 V with the RF signal of an 800 mV peak-to-peak voltage. A Keysight 81606A tunable laser source (TLS) sends light at 1478 nm into a bus of 17 cascaded modulators. The light, modulated by the modulator at corresponding resonance, goes through an erbium doped fiber amplifier (EDFA) before being measured by a Keysight N1092C sampling oscilloscope, with a Thorlabs EVOA1550A variable optical attenuator (VOA) placed before the optical input. The oscilloscope receives a clock trigger directly from the PPG and is set to pattern lock on the 16 Gbps NRZ PRBS15 pattern. Fig. 8d shows a completely open eye diagram captured by the oscilloscope with OMA ≈ 161.5 µW, demonstrating high promise for achieving the target 1 Tbps/fiber data rate at ultra-low energy.

Interleaved Contact Modulator Characterization The interleaved contact microdisk modulators are fabricated and characterized in the form of standalone test structures (Fig. 9a). As detailed in [56], the optimized design achieves ER = 36.5 dB, Q ≈ 6000, and FSR = 27.15 nm, with higher-order modes suppressed across the full C-band. With contact resistance further reduced through greater parallelism, we verified the improved RC bandwidth with an open eye diagram obtained at 32 Gbps, driven by PRBS15 signals with as low as 800 mV Vpp. The results are cross-validated with S11

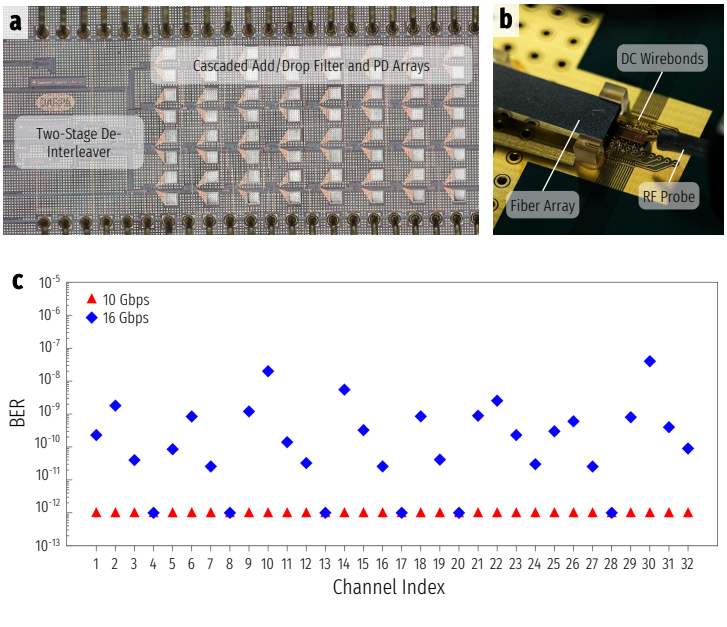

Figure 10. (a) Die photo of the 32-channel wire-bonded and optically packaged receiver chip featuring a two-stage de-interleaved multi-FSR architecture. **(b)** Optically packaged and DC wire-bonded receiver chip. **(c)** BER measurements for all 32 channels on the chip at both 10 Gbps and 16 Gbps [20, 59].

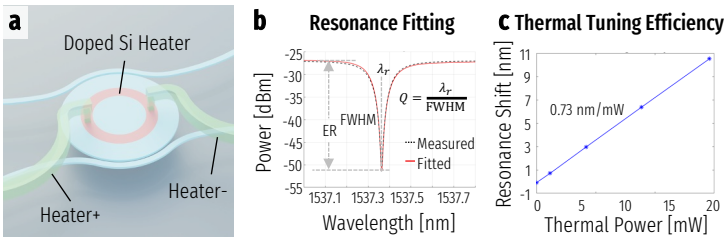

Figure 11. (a) Custom microdisk filters featuring conformal couplers and an integrated doped silicon heater have demonstrated exceptional suppression of higher order modes, while matching the modulator's resonance and dispersion behavior. **(b)** A representative filter spectrum showing key optical parameters for extractions. **(c)** Thermal tuning efficiency of the microdisk filters extracted as 0.73 nm/mW.

measurements, as shown in Fig. 9c, where the interleaved contact design results in significantly reduced back reflections compared to the quadrant design. This novel implementation of vertical-junction microdisk modulators thus provides a viable path toward achieving 100 Tbps escape bandwidth in a package similar to what conceived in Fig. 2d, by providing a double-folded data rate per channel at the same driving voltage.

3.3. Resonant Filter Arrays

Microresonator-based filter arrays perform channel-selective filtering of the modulated signal onto individual PDs for converting it back to the electrical domain. In light of the multi-FSR regime, the same de-interleaving structure can be employed to subdivide the channels onto separate banks of resonant filters for detection. In [20, 59], we have built a proof-of-concept 32-channel receiver chip, featuring two stages of de-interleavers and 4 buses of eight-channel add/drop ring filter arrays, optically packaged and DC wire-bonded. The receiver chip achieves natively error-free operation for all channels at 10 Gbps and for out of 32 channels at 16 Gbps, with anticipated improvement in receiver sensitivity by closely integrating with a transimpedance amplifier.

In addition to validating the symmetric link architecture, we also pushed along the device customization frontier by exploring custom microdisk filters. Addressing one of the design emphases of the link architecture in this study, namely the energy efficiency, microdisk filters are desirable due to

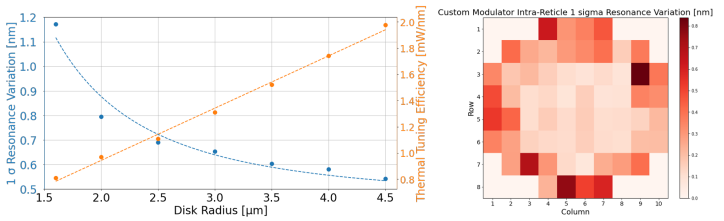

Figure 12. (a) 1 σ resonance wavelength variation as function of disk radius. 448 resonator devices in total were measured across 64 reticles. Wafer-scale average thermal tuning efficiency is also shown in units of mW/nm to emphasize the inverse relationship with 1 σ variation. **(b)** Intra-reticle resonance variation of custom microdisk modulators across wafer. Row and column indicated reticle location on wafer.

their inherent robustness to process variations [60], as well as an increased FSR upper bound that allows for a greater link design space. As illustrated in Fig. 11a, our custom microdisk filters are designed with conformal couplers and an integrated doped silicon heater that demonstrably suppress higher order modes [27]. We characterized the optical specifications of these custom microdisk filters following the same procedure as the quadrant modulators. Key optical specifications were extracted, including $Q \approx 11\,000$, FWHM $= 0.14$ nm, and ER $= 23$ dB. These measured optical specs are inline with the anticipated design values, providing the optical bandwidth required by a dedicated EIC to detect and recover the RF signal dropped by the filter. We also extract the thermal tuning efficiency of the custom filters to be 0.73 nm/mW. The custom filters have a greater thermal tuning efficiency than the modulators mainly due to the lack of an oxide barrier between the heater and the RF circuitry, which is required by the modulators for electrical isolation. In addition, the integrated heater of the filters features a radial shape that is closer to the optical mode, and less metal is present in the vicinity of the heater that would otherwise conduct heat away from the resonator device.

4. Process Variation and Energy Estimation

Critical to limiting energy consumption, our architecture benefits significantly from process-tolerant devices and integration of wafer-scale substrate undercut. In this section, we present measured wafer-scale process variations of our constituent devices, thermal tuning efficiency improvement from substrate undercut, and the associated implications on energy efficiency.

4.1. Wafer-Scale Process Variations

Custom add-drop microdisk filters over a range of radii from 1.6 μm to 4.5 μm were fabricated on a dedicated 300 mm wafer run through AIM Photonics, offering us the ability to collect comprehensive reticle-to-reticle statistics. Fig. 12a shows the effect of variation in fabrication on resonances of a particular microdisk measured across 64 reticles. Microdisks do not have an inner waveguide wall, giving them one less dimension affected by variations in fabrication than microring filters. Decreased variation in fabrication, which is inversely proportional to radius, leads to reduced need for thermal tuning to offset fabrication variation-induced resonance shift. Wafer-scale measurements indicate a linear relationship between radius and mW/nm tuning efficiency, and a reciprocal relationship between radius and 1 σ resonant wavelength variation due to variations in fabrication [61]. We also demonstrate a wafer map of intra-reticle variations in resonant wavelength of our custom modulators, shown in Fig. 12b, indicating the resonant devices are robust to process variations at both the wafer-scale and locally.

4.2. Wafer-Scale Substrate Undercut

Substrate undercut is a promising technique to reduce the thermal tuning energy required for rectifying the fabrication variations [40]. We have worked with our foundry partner, AIM Photonics, to co-develop a wafer-scale substrate undercut process. Due to the experimental nature of the process, and thus the stringent design rules keeping the undercut area away from the active

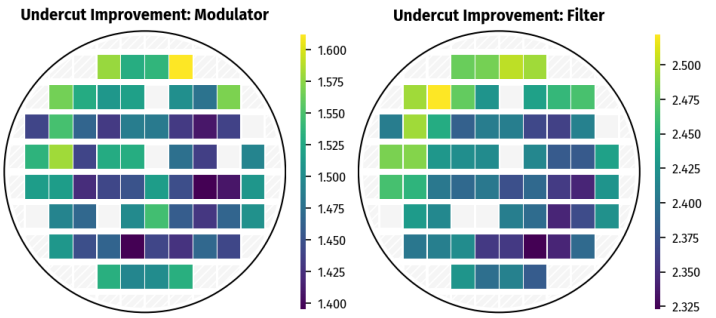

Figure 13. Measured thermal tuning efficiency improvement across wafer from wafer-scale substrate undercut. Up to ~1.6x and ~2.5x improvements are observed for disk modulators and filters, respectively.

devices by certain distances, the effectiveness of the process is expected to vary across the wafer and also depend on device layout. In Fig. 13, we show the measured improvement in thermal tuning efficiencies across the entire 300 mm wafer for both disk modulators and filters. The improvement is quantified by the ratio of the thermal tuning efficiency with and without substrate undercut. For disk modulators, the recorded improvement is up to ~1.6x, while for disk filters, the improvement can be extended to ~2.5x. This is likely due to the fact that the disk filters have less metal traces in the vicinity of the heaters, allowing for larger undercut area, and meanwhile, having fewer heat sinks that can potentially harm the thermal efficiency. In order to further improve the undercut effectiveness, future designs will look into optimizing metal contact and trace layouts in relation to the undercut area.

4.3. Energy Efficiency Implications

With latest knowledge of wafer-scale process variation magnitudes and effectiveness of substrate thermal undercuts, we estimate the thermal energy consumption for control of most constituent devices within the link. Integrated micro-heaters are used for either of the dual rings of the Kerr comb for initialization and stability. Previously fabricated integrated Kerr combs indicate a thermal energy consumption of 49–100fJ/b. We note that each 1.024 Tbps link consists of 9 (de-)interleavers, where each (de-)interleaver contains 3 thermo-optic phase shifters for the RAMZI arm, the assistive ring, and the monitoring MZI arm, respectively. These integrated heaters, as shown in Fig. 4, are necessary for interleaver alignment and flat-top response. The disk modulators and filters also utilize integrated heaters, as shown in Figs. 7 and 11, respectively, to achieve high-efficiency thermal tuning. Based on the latest characterization of wafer-scale process variations and tuning efficiencies, and assuming a 3σ design offset below the target values for the resonant devices, we derive Table 1 that summarizes the anticipated thermal energy consumption of the transceiver PIC. The anticipated improvement in tuning efficiency with substrate undercut for the Kerr comb and interleavers are based on the data point from the microdisk filters, due to its geometry design being the most friendly to undercut placement. We will continue to work toward improving the effectiveness of substrate undercuts, and thus the energy efficiency of the link, through a co-design of device and undercut geometries.

5. Conclusion and Future Work

In conclusion, we have presented the design and characterization of a groundbreaking Kerr comb–driven SiPh DWDM transceiver chip, which offers a scalable architecture for ultra-high bandwidth and energy-efficient die-to-die connectivity. Our results demonstrate the feasibility of achieving a chip shoreline bandwidth density of over 2 Tbps with a sub-pJ/b energy consumption, which is significant in the context of exponentially growing traffic demands in data centers and high-performance computing systems. The multi-FSR regime adopted in this work enables the utilization of microresonators with moderate FSR for ultra-broadband DWDM with minimal crosstalk penalties. The preliminary characterization of crucial components such as the even-odd (de-)interleavers and microresonator modulators and filters has laid the groundwork for subsequent system-wide validations.

Table 1. Expected thermal energy consumption of both constituent components and total link, obtained by dividing the expected power dissipation by the link data rate. The expected energy efficiency for devices with substrate undercuts is also listed based on latest characterization results.

Component	w/o Undercuts	w/ Undercuts
Comb Source [fJ/b]	49 – 100	19.6 – 40
(De-)Interleavers [fJ/b]	70	28
Disk Modulators [fJ/b]	329	206
Disk Filters [fJ/b]	149	59.6
Total Thermal Energy [fJ/b]	597 – 648	313.2 – 333.6

For future work, we aim to further enhance the modulator and filter designs to substantially boost the chip escape bandwidth. Link-level demonstrations will be carried out to validate the transceiver's performance systematically. With a focus on mitigating the impact of process variations and maximizing energy efficiency, future designs will also look into improving the effectiveness of wafer-scale thermal undercuts and adopting fabrication-robust device designs. The progress made in this study is a key step towards realizing the vision of seamlessly integrated photonics and electronics in future computing systems.

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