Reconfigurable Silicon Photonic Transceiver for Space-Based Communication Nodes

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(Invited Paper)

***Abstract*—The surge in deployment of Low Earth Orbit (LEO) satellites over the last two decades has resulted in a number of incompatible communication protocols, limiting efficient inter-satellite communication. In response, we present the first reconfigurable silicon photonic link supporting both coherent and intensity modulation with direct detection (IM-DD). Our link design supports transmission and reception of on-off keying (OOK), binary phase-shift keying (BPSK), and quadrature phase-shift keying (QPSK) modulated signals across two polarization states, enabling a single transceiver to accommodate multiple common modulation formats. We demonstrate successful operation of the custom transmitter, polarization multiplexer, and receiver portions of our link, including: 1) transmission of OOK, BPSK, and QPSK at symbol rates up to 10 GBaud with an error vector magnitude (EVM) $<$ 22% in all cases, 2) polarization cross-talk suppression of over 21 dB, and 3) reception of OOK, BPSK, and QPSK at rates up to 5 GBaud with resolved EVM $<$17%. This innovation can address the pressing need for standardized communication within LEO satellite constellations, improving interoperability and efficiency in satellite communications.**

***Index Terms*—Optical communication, optical modulation, optical polarization, optical receivers, optical waveguides, phase shift keying, quadrature phase shift keying (QPSK), satellite communication.**

I. Introduction

OPTICAL wireless communications (OWC) have become essential in modern telecommunications, enabling widespread access to high-speed connectivity in a variety of application spaces [1]. In recent years, there has been growing interest in utilizing near-infrared (NIR) OWC to replace or complement radio-frequency (RF) communications in applications such as ground-to-space, satellite-to-satellite, and underwater communications [2]. NIR coherent communications have already been growing in popularity for terrestrial applications, due to their high spectral efficiency and per-channel bit rate [3]. As NIR beam propagation is close to 50% faster in vacuum compared to optical fiber, OWC has become an attractive area to deploy coherent communication techniques. OWC using these wavelengths is well-suited for applications with ultra-long distances between the transmitter and the receiver [4], [5]. Specifically, OWC has proven to be particularly attractive for inter-satellite communication for low-earth orbit (LEO) satellites due to the demanding requirement for low latency, ultra-long distance communication [6].

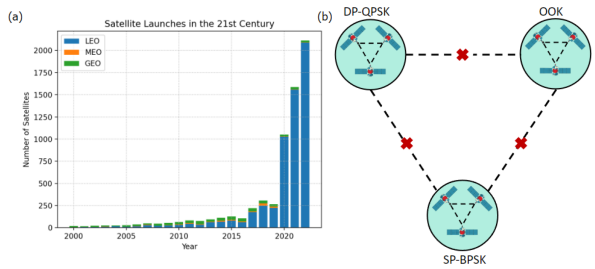

Fig. 1. (a) Satellite launches since 2000; LEO satellites are experiencing exponential growth in deployment. (b) Example of LEO constellation communication incompatibility due to mismatched modulation formats.

In just the past decade, three of the most notable active LEO constellation operators – Starlink, Telesat, and OneWeb – deployed 4,425, 117, and 720 LEO satellites, respectively [7]. Additionally, SpaceX has proposed a 12,000 unit mega constellation of Starlink LEO satellites [8]. As seen in Fig. 1, there has been an exponential growth in the number of such deployments over the last two decades [9]. However, the novelty of many of these systems has led to the emergence of numerous incompatible communication standards with respect to modulation rate, format, and multiplexing [10]. These discrepancies prevent satellites from effectively communicating with each

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TABLE I
NOTABLE INTER SATELLITE LINKS OF THE 21ST CENTURY, HIGHLIGHTING A MISMATCH IN COMMUNICATION STANDARDS

Modulation Standard	Format	Data Rate	Reference
PPM	IM-DD	622 Mbps	[13]
NRZ	IM-DD	10.7 Gbps	[14]
BPSK	Coherent	1.8 Gbps	[15]
QPSK	Coherent	10 Gbps	[16]
DP-QPSK	Coherent	10 Gbps	[17]

other, posing a bottleneck to achieving more widespread connectivity. Table I summarizes some recent inter-satellite links, which exemplifies this issue of incompatible standards. We note that there has been increased interest in both coherent and intensity modulated standards for use in space-based OWC [11], [12].

A solution to this bottleneck is the Optical Inter-Satellite Link (OISL). An OISL must possess the ability to transmit and receive various protocols for both intensity and coherent modulation, in order to facilitate effective communication between heterogeneous links. To address this critical need, we previously introduced the first fully reconfigurable, dual-polarization silicon photonic transceiver capable of transmitting and receiving both coherent and intensity modulation. Our abstract at OFC '24 [18] and invited talk at OFC '25 [19] provided a brief overview of the overall architecture and presented preliminary results from the operation of the transmitter. This manuscript describes the architecture of the full transceiver in greater detail and presents updated results from the transmitter, polarization multiplexer/demultiplexer, and receiver. Here we are focused exclusively on the on-chip device performance, with an eye towards meeting the aforementioned demands of heterogeneous satellite protocols.

Specifically, for the transmitter, we report a successful reconfigurable transmitter design capable of outputting OOK, BPSK, and QPSK signals at symbol rates up to 10 GBaud with EVM less than 22%. For the polarization multiplexer/de-multiplexer, we report an on-chip, all-silicon device capable of demultiplexing mixed-polarization light into separate TE channels with polarization cross-talk suppression of over 21 dB. Finally, for the receiver, we report a PDK-based 90° hybrid structure that receives OOK, BPSK, and QPSK signals at 5 GBaud, with EVM no greater than 17%.

The rest of this manuscript is organized as follows. First, we describe the architecture and theory of operation for the transmitter, polarization multiplexer/de-multiplexer, and receiver. Then, we discuss how the architecture supports self-calibration, and describe how reconfiguration between data formats is physically achieved. Finally, we present results for the operation of each component, demonstrating how our system can address the aforementioned requirements of space-based OWC systems.

II. TRANSCEIVER ARCHITECTURE

The entire transceiver circuit is located on a single photonic integrated circuit (PIC) chip, where it can be subdivided into two sections: transmitter and receiver. It is critical that the transceiver occupies this single PIC, as it allows integration with a single electronic integrated circuit (EIC) to form the complete OISL. The transmitter modulates an optical signal according to the destination format and consists of two polarization paths, each containing a reconfigurable IQ modulator. This IQ modulator generates an in-phase and a quadrature component which together form a complex-amplitude waveform according to the programmed modulation format. Each IQ modulator can be operated independently in order to produce a single or dual-polarization version of the desired signal. The transmitter terminates with a polarization splitter/rotator (PSR) which multiplexes the two polarization channels together for off-chip transmission. The receiver decodes a signal according to the source format. It begins with the same PSR device operating now as a de-multiplexer, sending each channel to a separate 90° hybrid for signal reception. Our architecture is designed for compatibility with standard silicon-on-insulator (SOI) foundry processes. Fig. 2 illustrates the overall system design of our reconfigurable photonic circuit.

The transmit path begins with light generated by a continuous-wave (CW) laser. This light is injected into the PIC through a polarization maintaining fiber (PMF), which ensures that the polarization of the light remains stable as it enters the chip. This is essential as our photonic devices are optimized for performance with the fundamental TE mode. On the edge of the PIC, in order to efficiently couple both TE and TM light for dual-polarization signals, we use undercut silicon nitride edge couplers for low-loss operation [20]. Once coupled inside, the light is directed toward one or both polarization channels using a 2×2 Mach-Zehnder Interferometer (MZI) switch. This MZI switch can be thermally configured to either direct the light into a single polarization channel (X or Y) or split it between both, allowing for either single or dual polarization operation. The MZI itself is controlled via undercut thermo-optic (TO) phase shifters to achieve a high thermal efficiency [21]. The key modulation elements for both transmit paths are IQ modulators, each built using two traveling wave Mach-Zehnder modulators (TW-MZMs) in the push-pull driving configuration. TW-MZMs are widely used in high-speed coherent optical systems because they can handle high data rates and provide precise phase and amplitude control [22]. Our MZMs utilize a reverse-biased lateral PN junction in order to modulate at frequencies up to 20 GHz. The bias states of the parent and child MZMs are controlled using the aforementioned TO phase shifters, which reconfigure the modulation format.

Following this, a PSR is used to manage the recombination of signals from the different polarization paths. The output of the Y-polarization path's IQ modulator is rotated from TE to TM polarization, while the output of the X-polarization path's IQ modulator is maintained as TE-polarized light, resulting in two orthogonal signals. The complete transmit signal is coupled off-chip into the PMF.

On the receiver side, the inbound signal is first directed into the combined port of a PSR, where the reverse operation occurs. The TE-polarized signal is maintained as TE polarization, and is routed to the X-polarization path. The TM-polarized signal is rotated to the TE polarization, and routed to the Y-polarization path. In parallel, light is coupled onto a chip from a separate laser serving as the local oscillator (LO). Following the receiver

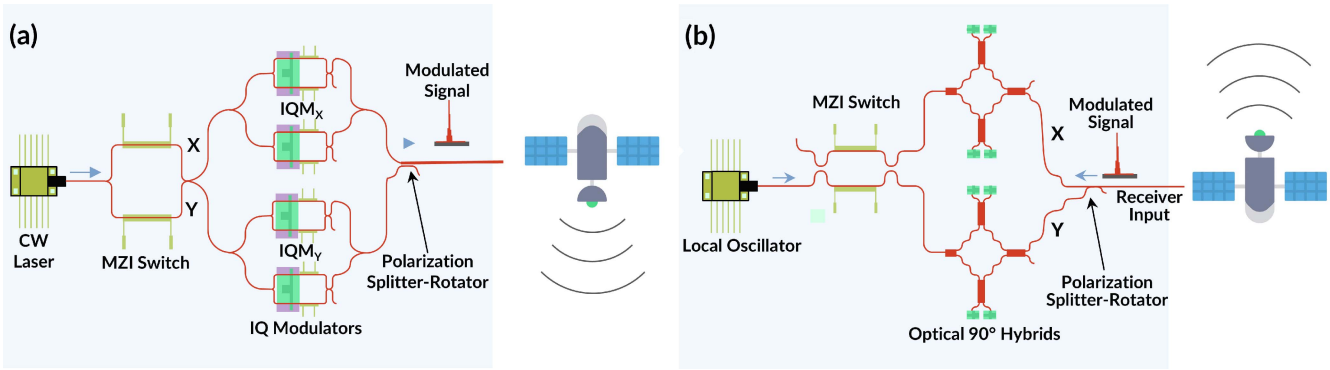

Fig. 2. (a) Schematic of the reconfigurable transmitter capable of dual-polarization coherent and intensity modulation (b) Schematic of the reconfigurable receiver capable of decoding dual-polarized coherent or intensity modulated signals.

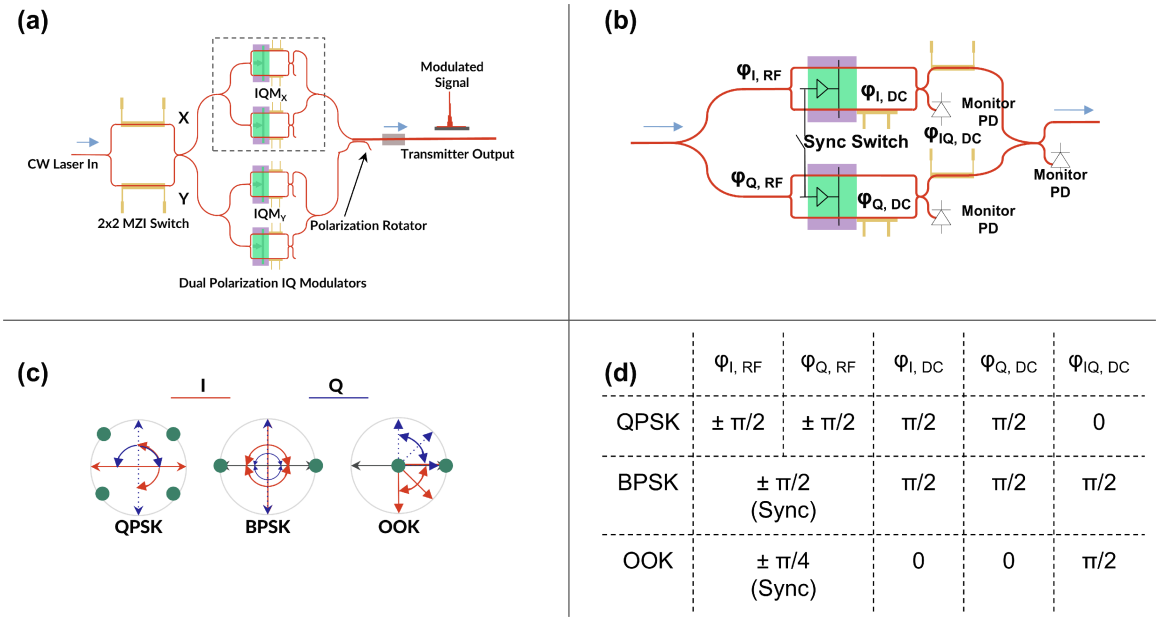

Fig. 3. (a) Full transmitter schematic for dual polarization operation. (b) Single reconfigurable IQ modulator for coherent and intensity modulated signals. (c) Phase representation of different formats. (d) Operating points for different formats.

polarization de-multiplexing, the signal is mixed with the LO inside of a compact 90° hybrid, which is terminated with two pairs of photodiodes. These photodiodes output four currents to off-chip trans-impedance amplifiers (TIA's), which amplify the difference between the currents in each pair, producing an in-phase and a quadrature electrical signal. These two signals are then read by digital-signal processing (DSP) software in order to decode the modulated data.

III. Transmitter Operating Principle

Our architecture supports three of the most common modulation formats: On-Off Keying (OOK), Binary Phase Shift Keying (BPSK), and Quadrature Phase Shift Keying (QPSK). Both polarization channels (X and Y) can be programmed independently to any of these three modulation formats, resulting in single or dual-polarization variants of each. The key enabling technology in our architecture is the customized IQ modulator, which is built using two identical child MZMs nested into a parent MZM with an additional phase control switch. Fig. 3(a) shows a schematic of the full transmit path.

The optical path of an individual IQ modulator can be seen in Fig. 3(b). Light enters the parent MZM and is divided evenly between the I and Q branches via a Y-splitter. On each branch, the light then enters the respective child MZM, where it is again split evenly via a Y-splitter. When propagating through an arm of the child MZM, the phase can be delayed by an RF electro-optic (EO) phase shifter, then by a TO phase shifter. The upper and lower branch EO phase shifters each apply a phase of $\pm\phi_{I/Q,RF}$, while the TO phase shifters apply a net phase difference of $\phi_{I/Q,DC}$. In order to minimize the phase shift needed, we apply $\phi_{I/Q,DC}$ on the lower arm of the child MZM (the cross-port relative to the signal output). After the phase shifts are applied, the light from the upper and lower branches

is recombined in a 2×2 multi-mode interferometer (MMI) coupler, where constructive or destructive interference of the electric fields occurs. One MMI output returns the signal to the parent MZM path, and the other sends the inverted optical signal to a monitor photodiode. Within the parent MZM, the light on either branch may be delayed by a final TO phase shifter. The net phase difference applied between the I and Q branches is $\phi_{IQ,DC}$, also called the phase bias. We apply the phase bias on the TO phase shifter located on the I branch in order to minimize the necessary phase shift. Finally, the light from the I and Q branches are interfered in another MMI, where one output sends the modulated signal onto the main transmit path, and the other output sends the inverted signal to a monitor photodiode.

The combined output of the reconfigurable IQ modulator can be expressed as:

$$E_{\text{out}}(t) = \frac{E_0}{4}\Big[(e^{j(\phi_{IQ,DC})})(e^{j(\phi_{I,RF})} + je^{j(\phi_{I,DC}-\phi_{I,RF})}) + j(e^{j(\phi_{Q,RF})} + je^{j(\phi_{Q,DC}-\phi_{Q,RF})})\Big] \quad (1)$$

Our design utilizes balanced MZM's in the push-pull configuration, a design where a positive or negative phase shift can be placed on either arm relative to the initial bias point. To begin, the PN junction on both arms is held at identical DC reverse bias, which maintains a consistent starting phase. Then, an RF signal $\phi_{I/Q,RF}$ is applied to the top arm, and its inverse is simultaneously applied to the bottom arm. When the amplitude of this signal is positive, the phase on the upper arm is increased (a positive phase shift), while the negative amplitude on the bottom arm decreases the phase. Operating in this fashion allows us to reduce the phase needed on any particular arm by half, thereby reducing the driver swing as well, compared to single-ended operation. This is critical for our design, which is intended to be driven by CMOS electrical drivers.

A. On-Off Keying (OOK)

During OOK modulation, the electric field output from each child MZM oscillates between 0 and E_0, and the electrical data on the I and Q branches are synchronized, leading to constructive interference in the parent MZM. In order to achieve this, the initial state of the child MZMs should be set to transmit $E_0/\sqrt{2}$, with the high-speed data signal causing $\phi_{I/Q,RF}$ to oscillate between $-\pi/4$ and $+\pi/4$. The 2×2 coupler applies an inherent $\pi/2$ phase shift to the cross-branch signal, so we do not need to apply bias to either TO phase shifter, and $\phi_{I/Q,DC}$ is therefore equal to 0. When $\phi_{I/Q,RF}$ is equal to $+\pi/4$, the relative phase of the top branch becomes equal to that of the bottom branch, leading to constructive interference and an output electric field of E_0. When $\phi_{I/Q,RF}$ is equal to $-\pi/4$, the phase of the bottom branch relative to the top branch becomes π, leading to destructive interference and an output electric field of 0. The sync switch is closed so that the same electrical waveform modulates the I and Q branches. The MMI of the parent MZM causes I and Q to inherently be out of phase by $\pi/2$. $\phi_{IQ,DC}$ is set to $\pi/2$ to compensate, and the in-phase I and Q branch signals constructively interfere.

The combined electric field output can then be written as:

$$E_{\text{out}}(t) = E_0(e^{j\frac{3\pi}{4}})\left[\cos(\phi_{RF}(t) - \pi/4)\right] \quad (2)$$

where $\phi_{RF}(t) = \phi_{I,RF}(t) = \phi_{Q,RF}(t)$, and $e^{j\frac{3\pi}{4}}$ is a global phase shift which can be neglected.

B. Binary Phase Shift Keying (BPSK)

During BPSK modulation, the electric field output from each child MZM oscillates between $-E_0$ and E_0, and the electrical data on the I and Q branches are once again synchronized, leading to constructive interference in the parent MZM. To achieve phase modulation, the initial state of the child MZMs should be set to transmit an electric field equal to 0, with the high-speed data signal causing $\phi_{I/Q,RF}$ to oscillate between $\pi/2$ and $-\pi/2$. The inherent $\pi/2$ phase shift of the 2×2 coupler is not sufficient for full extinction, so we now must apply a bias to the lower arm's TO phase shifter, and $\phi_{I/Q,DC}$ is now equal to $\pi/2$. When $\phi_{I/Q,RF}$ is equal to $+\pi/2$, the relative phase of the top branch becomes equal to that of the bottom branch, leading to constructive interference and an output electric field of E_0. When $\phi_{I/Q,RF}$ is equal to $-\pi/2$, the phase difference between the bottom branch and top branch becomes -2π, leading to constructive interference and an output electric field of $-E_0$. The sync switch is closed so that the same electrical waveform modulates the I and Q branches. The MMI of the parent MZM causes I and Q to inherently be out of phase by $\pi/2$. $\phi_{IQ,DC}$ is set to $\pi/2$ to compensate, and the in-phase I and Q branch signals constructively interfere.

The combined electric field output can then be written as:

$$E_{\text{out}}(t) = E_0\left[\sin(\phi_{RF}(t))\right] \quad (3)$$

where $\phi_{RF}(t) = \phi_{I,RF}(t) = \phi_{Q,RF}(t)$.

C. Quadrature Phase Shift Keying (QPSK)

During QPSK modulation, the electric field output from each child MZM oscillates between $-E_0$ and E_0, but now the electrical data on the I and Q branches are fed from separate, uncorrelated sources. The child MZM settings are the same for phase modulation as in the BPSK case. The initial state of the child MZMs should be set to transmit an electric field equal to 0, so we set $\phi_{I/Q,DC}$ equal to $\pi/2$. $\phi_{I/Q,RF}$ is again equal to $\pm\pi/2$. The sync switch is now open, because the I and Q branch data is uncorrelated. The MMI of the parent MZM causes the branches to inherently be out of phase by $\pi/2$, which is desired to produce orthogonal I and Q phasors. As such, $\phi_{IQ,DC}$ is set to 0.

The combined electric field output can then be written as:

$$E_{\text{out}}(t) = \frac{E_0}{2}\left[\sin(\phi_{I,RF}(t)) + j\sin(\phi_{Q,RF}(t))\right] \quad (4)$$

D. Single and Dual Polarization

As mentioned before, for all three modulation formats, our architecture supports both single and dual-polarized signals. For this, we use a 1×2 MZI switch to direct light into one or both of the IQ modulators. By default, the inherent $\pi/2$ phase shift

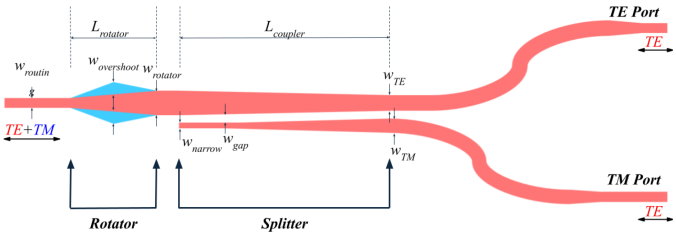

Fig. 4. Custom PSR schematic, showing adjustable design parameters, and modes physically present at each port. The red regions denote full-height Si, and the blue regions denote half-height Si.

of the MMI cross-port causes the input power to be split evenly between the X and Y paths, so for dual polarization we do not need to apply any phase to the switch. For single-polarization, we apply a bias of $\pi/2$ to the corresponding bar heater, in order to match the inherent bias on the cross port: we apply bias to the top heater for the X polarization path, and the bottom heater for the Y polarization path.

Fig. 3(c) shows a visual representation of the phasors for each modulation, and Fig. 3(d) summarizes the required settings for each case.

IV. Polarization Multiplexing

Employing multiple polarization states allows us to increase the data rate of a link by a factor equal to the number of polarization states used. With dual polarization, this allows us to double the data rate of the link by interleaving the data sent across two modulation paths. Alternatively, as the two polarization states are orthogonal, and therefore do not interfere with one another, we can send uncorrelated data in parallel using the same optical pathway. A practical OISL benefits greatly from possessing dual-polarization capability.

The rectangular silicon and silicon nitride waveguides used in standard foundry processes support both TE and TM polarized light, but the asymmetry of the waveguides leads to birefringence, causing differences in the performance of devices between the respective polarization states. It is usually impractical to design for the phase differences between TE and TM light in the same structure; since TE light is more confined, most devices tend to be optimized exclusively for TE operation [23]. In our architecture, the signals on both polarization paths are TE-polarized until they reach the chip edge. Then, in order to perform polarization multiplexing (in the transmitter) and de-multiplexing (in the receiver), we employ a custom silicon waveguide-based PSR that is foundry-compatible and compact. This device, seen in Fig. 4, consists of two sections: the polarization rotator, which rotates the TM0 mode to the TE1 mode via mode hybridization [24], and the polarization splitter, which couples the TE1 mode in the central waveguide to the TE0 mode of a parallel waveguide, physically isolating the X and Y signals. This process also works in reverse.

A. Polarization Rotator

Mode hybridization occurs when there is an asymmetry in the waveguide structure along either the vertical or horizontal axis. When we break the cross-sectional symmetry, it causes the effective index values of certain modes to approach each other at a certain waveguide width. Near that width, the modes become nearly indistinguishable. If the waveguide is tapered from slightly less than that width (where the TM0 index is higher), to slightly more than that width (where the TE1 index is higher), the TM0 mode will evolve into the TE1 mode as it propagates. At the same time, the input TE0 mode (which possesses a higher effective index) will not be affected [25].

Our design is based on [26], adapted for the chosen foundry process. It uses a ribbed Si waveguide, with a central 210 nm tall waveguide rib surrounded by a 105 nm tall half-etched ridge that breaks the vertical symmetry, causing mode hybridization. The central rib is adiabatically tapered from an initial width (w_{routing}) of 450 nm to a width (w_{rotator}) of 850 nm over a length (L_{rotator}) of 100 μm, while the ridge overshoot tapers from 0 nm to a maximum overshoot ($w_{\mathrm{overshoot}}$) of 500 nm on either side, before tapering back to 0 nm overshoot.

B. Polarization Splitter

Following the rotator, an adiabatic asymmetric coupler serves as the polarization splitter. The widened central waveguide supports orthogonal TE0 and TE1 modes with different effective indices. A second, narrower waveguide is brought in next to it with a coupling gap (w_{gap}) of 200 nm. This waveguide does not support the higher-order TE1 mode. Over the 300 μm length of the coupling region (L_{coupler}), the narrow waveguide is tapered up to a final width (w_{TM}) of 500 nm while the central waveguide is tapered down to a width (w_{TE}) of 650 nm. The tapering of the two waveguides is matched such that the coupling gap remains constant. The evolution of the TE0 and TE1 supermodes causes the TE1 mode to couple into the TE0 mode supported by the second waveguide, while the TE0 mode in the central waveguide self-couples, causing the energy to remain on the main path. S-bends direct the waveguides away from one another in order to avoid any further coupling. We call the output of the central path the "TE Port" and the output of the second path the "TM Port".

We designed our PSR by performing parameter sweeps of L_{rotator} and L_{coupler} in Tidy3D's Finite-Difference Time Domain (FDTD) solver. For our design, we are most interested in minimizing the crosstalk between modes. To that end, we compare the power measured on the output port corresponding to the input mode with the power measured on the opposite port. The ratio between these values is the polarization extinction ratio. From simulation, we expected a TE extinction ratio at the TM Port of 44 dB at 1550 nm, and a TM extinction ratio at the TE Port of 25 dB.

In [27] it was demonstrated that for a polarization extinction ratio of at least 20 dB the sensitivity power penalty in a coherent receiver approaches zero. As our design's extinction ratio was at least 25 dB, these expected values enable us to achieve the minimum BER for a given signal power, and are thus considered acceptable.

V. Receiver Operating Principle

The receiver portion of our architecture supports all of the modulation formats produced by our transmitter, in single- or

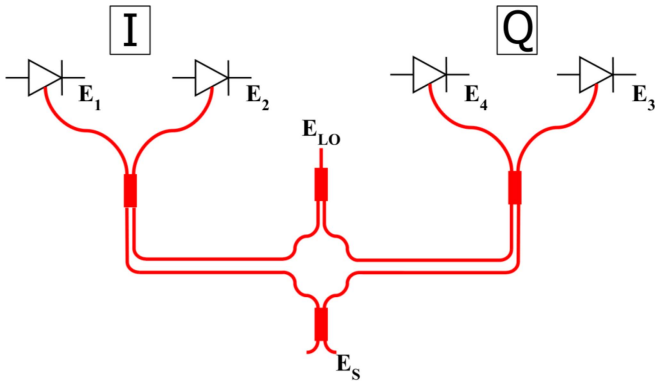

Fig. 5. Coherent receiver 90° hybrid schematic.

dual-polarization configurations. We utilize an intradyne receiver, which allows us to measure both the in-phase (I) and a quadrature (Q) components because it maintains the full information of the complex amplitude [28]. This type of device has four outputs, where the electric fields of the LO and signal are out of phase relative to each other by 0°, 90°, 180°, or 270°. The 0° and 180° outputs form the I branch, while the 90° and 270° outputs form the Q branch. These outputs are each received by a photodiode that converts them into a current. The current pairs on each branch are subtracted to form the in-phase and quadrature components of the electrical signal [29]. In our architecture, the enabling receiver technology is the compact 90° hybrid, one of which is present on each polarization path following the PSR demultiplexing.

A schematic of our 90° hybrid design can be seen in Fig. 5. It follows the one described in [30], consisting of discrete 1×2 and 2×2 couplers. This architecture was chosen as it can be constructed entirely from well-characterized PDK components, and does not rely on custom device designs. The LO light enters the structure at E_{LO}, where it is split between the I and Q branches by a 1×2 MMI splitter. The received signal enters at E_S, where a 2×2 MMI coupler divides it between the I and Q branches, imparting a $\pi/2$ phase shift on the signal headed to the I branch. A second 2×2 MMI coupler serves as the end of both the I and Q branches, where the LO and signal are mixed, with a $\pi/2$ phase shift imparted to the light on the cross-coupled path. The resulting power is split between a pair of PD's. The PD's convert the electric fields of the light (E_1 and E_2, E_3 and E_4) into currents. The current from each pair is sent to a trans-impedance amplifier on a separate electronic chip, where the difference between the PD currents is taken and converted to a new current value that is interpreted by digital signal processing (DSP).

The resulting electric fields from the structure can be written as:

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \\ E_4 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} E_S + E_{LO} \\ E_S - E_{LO} \\ E_S + jE_{LO} \\ E_S - jE_{LO} \end{bmatrix} \tag{5}$$

The PD current is simply the product of the PD responsivity R and the amplitude of the incident electric field E:

$$I(t) = R * |E(t)|^2 \tag{6}$$

As these are PDK devices co-located on the same PIC, we assume all PD's possess the same responsivity. Combining (5) and (6), we obtain:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \frac{R}{4} \begin{bmatrix} |E_S + E_{LO}|^2 \\ |E_S - E_{LO}|^2 \\ |E_S + jE_{LO}|^2 \\ |E_S - jE_{LO}|^2 \end{bmatrix} \tag{7}$$

The TIA's take the difference between currents at each branch:

$$I_I = I_1 - I_2 \tag{8}$$

$$I_Q = I_3 - I_4 \tag{9}$$

Plugging (7) into (8) and (9), and then simplifying, we obtain the I and Q branch signal equations:

$$I_I = R * E_{LO,0} * E_{s,0}(t) \cos(\phi_S(t)) \tag{10}$$

$$I_Q = R * E_{LO,0} * E_{s,0}(t) \sin(\phi_S(t)) \tag{11}$$

Where $E_{LO,0}$ is the local oscillator field amplitude, $E_{s,0}(t)$ is the amplitude modulation of the signal, and $\phi_S(t)$ is the phase modulation of the signal.

Equations (10) and (11) represent ideal hybrid outputs, where the phase imparted on each path between the first stage of splitters and the second stage of splitters is identical. In this 90° hybrid architecture it is critical for the waveguide paths from the first set of splitters to the second set of splitters to match in length, to maintain this relative phase. Our layout uses identical 90° waveguide bends and we match all waveguide path lengths. Despite this, unavoidable fabrication variations will cause slight differences in the accumulated phase in each path, resulting in phase error. If kept minimal, this error can be corrected using DSP [28], [29].

A. On-Off Keying (OOK)

In the case of OOK modulation, the phase of the signal is not modulated, only the amplitude. As such, $E_{S,0}(t)$ oscillates between 0 and E_0, and $\phi_S(t)$ is a constant, such that $I_Q = 0$. Therefore, $\phi_S(t)$ must equal 0°, and the new equations are:

$$I_I = R * E_{LO,0} * E_{s,0}(t) \tag{12}$$

$$I_Q = 0 \tag{13}$$

Unlike coherent phase-modulated signals, OOK signals can be detected with a single photodiode. However, as (12) and (13) demonstrate, our receiver, necessary for more complex phase modulation, can still detect an OOK signal. Further, using a balanced detector and LO offers some benefits over direct detection with a single PD, such as higher sensitivity from the added power of the LO, which serves as an effective on-chip preamplifier [31].

B. Binary Phase Shift Keying (BPSK)

In the case of phase modulation, the amplitude of the signal is not modulated, only the phase. As such, $\phi_S(t)$ oscillates between 0° and 180°, and now $E_{S,0}(t)$ is constant. The equations now become:

$$I_I = R * E_{LO,0} * E_0 * \cos(\phi_S(t)) \tag{14}$$

$$I_Q = R * E_{LO,0} * E_0 * \sin(\phi_S(t)) \tag{15}$$

In the BPSK case, there is no quadrature state, only an in-phase state. As such, $\phi_S(t)$ will only take on 0° and 180° as values.

C. Quadrature Phase Shift Keying (QPSK)

The QPSK case is also a phase modulation case, and as such, (14) and (15) are once again the governing equations. Unlike BPSK, there is now a quadrature state as well, with four total symbols. Now, $\phi_S(t)$ will take on four values: 0°, 90°, 180°, and 270°.

D. Single and Dual Polarization

As aforementioned, the outputs of the PSR go to two separate 90° hybrids, one for the X-polarization branch and one for the Y-polarization branch. The polarization of the LO is keyed to the TE axis and preserved by the PMF, so that it matches the TE polarization of the signals after they have been demultiplexed by the PSR.

VI. Calibration Control Loop

Our architecture enables calibration via integrated monitor PD's, which allows us to set the bias points for each modulation format, compensate for fabrication variations, and adjust the system in real-time based on environmental fluctuations such as temperature. As seen in Fig. 3(b), each MZM inside of the IQ modulators is terminated with a 2×2 MMI, and a monitor PD is placed on the cross output port to monitor the power of the inverse signal. TIA's then convert the photocurrents into voltage signals that can be read by an Analog to Digital Converter (ADC). There are three signals to monitor on each IQ modulator: the I and Q branch child MZM outputs, and the parent MZM output. We use the measured signal values to set the appropriate bias state during setup, and to adjust system performance during operation. We refer to the former as "static calibration" and the latter as "dynamic calibration."

A. Static Calibration

We perform static calibration immediately prior to transmitting a signal. The first step of static calibration is to adjust the polarization input switch for the appropriate polarization state, either single-polarization X, single-polarization Y, or dual-polarization. Next, we tune the parent MZM to obtain the correct I-Q phase offset, depending on whether we have a quadrature state or not. Then we tune each child MZM to the bias setting for either amplitude modulation or phase modulation, depending on the transmitted data format. Finally, we return to the previous bias steps and fine-tune the heater values for optimal performance. Although we have a known V_π value for our heaters, as well as known bias settings (see Fig. 3(d)), in practice it is necessary to make adjustments to compensate for fabrication variations or thermal fluctuations. Static calibration allows us to do so.

To select the correct polarization state, we observe the power measured by the parent MZM monitor PD's in both the X and Y paths. To obtain single-polarization operation on the X branch, we tune the top heater in the polarization control switch such that the power on the Y branch monitor PD is minimized. This informs us that power is sent entirely to the X branch. In contrast, to obtain single-polarization on the Y branch, we tune the bottom heater in the polarization switch to minimize the power at the X branch monitor PD. Lastly, dual-polarization operation is enabled without heater bias due to the 2×2 MMI in the polarization switch. However, to balance the X and Y branch power, we monitor both X and Y branches simultaneously, and make minute adjustments to either heater as necessary to match the power on each branch.

In the OOK case, the parent MZM must be set such that the I and Q branches are in phase (no quadrature), and the child MZM's must be set for amplitude modulation. For the parent MZM, we observe the output power on the parent MZM monitor PD, which is the cross-port of the signal output. We tune the TO phase shifter on the I branch ($\phi_{IQ,DC}$) such that the power measured is minimized, as this corresponds to full constructive interference of the I and Q branches on the opposite output port. For the child MZM's, the amplitude modulation setting requires the two arms of the phase shifter to be out of phase by $\pi/2$, leading to identical output power on both output ports. The 2×2 MMI's in each MZM should provide the inherent 90° phase shift required, but in reality, we may need to optimize with this using the integrated heaters. There are two options for how to optimize the data. The first is to use the received signal. Once data transmission has begun, we can adjust either heater of the child MZM as necessary to maximize the optical extinction ratio (ER) of the received signal. Alternatively, we can record the voltages that maximize and minimize power on the child monitor PD's, and interpolate a value that provides half of full power (the -3 dB point).

In the BPSK case, the parent MZM is once again set to keep I and Q in-phase, while the child MZM's are instead set for phase modulation. Like in the OOK case, we tune the I branch TO phase shifter to minimize power on the parent monitor PD. The phase modulation setting requires each child MZM to be set to its null point, where output power on the signal port is minimized. To tune each child MZM, we observe the power on the child monitor PD's. We tune the TO phase shifter on the lower arm of the MZM ($\phi_{I/Q,DC}$) such that the power measured is maximized, which corresponds to the null point of the signal port.

In the QPSK case, the parent MZM is now set to offset I and Q by 90°, while the child MZM's are set for phase modulation identically to the BPSK case. Similar to the child MZM's for OOK, the 2×2 MMI provide the 90° phase shift needed for the quadrature state, but we still may need to optimize the I-Q phase offset. To do this, we may follow one of the two aforementioned

TABLE II
SUMMARY OF STATIC CALIBRATION PROCEDURES

Format	Children MZM Setting	Children Monitor PD	Parent MZM Setting	Parent Monitor PD
OOK	Quadrature	Interpolate half-power	I and Q In-Phase	Minimize measured power
BPSK	Null Point	Maximize measured power	I and Q In-Phase	Minimize measured power
QPSK	Null Point	Maximize measured power	I and Q quadrature	Interpolate half-power

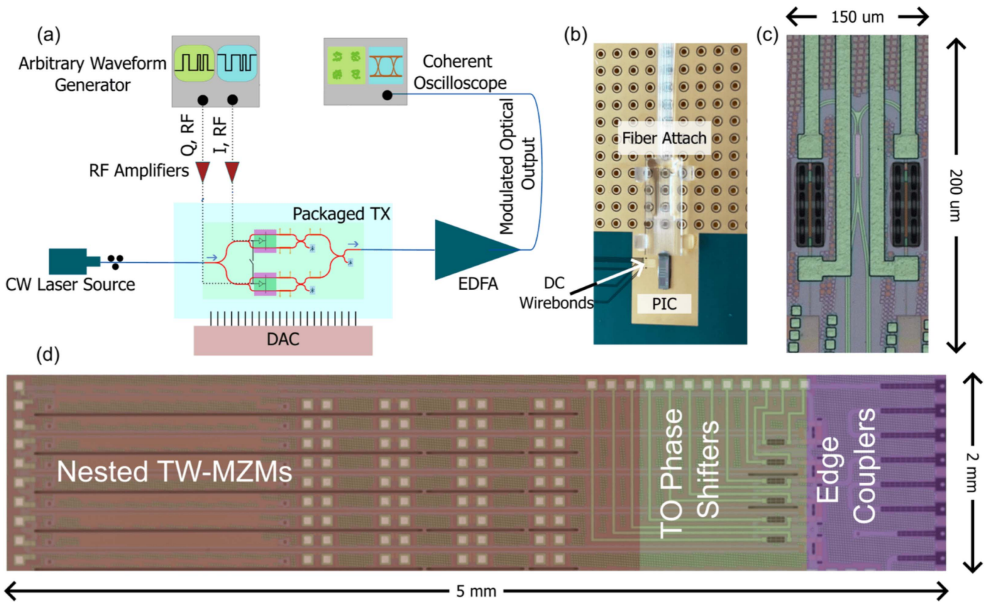

Fig. 6. (a) Full transmitter experimental setup. (b) Packaged PIC with DC wirebonds, die-attach, and fiber-attach. (c) Undercut TO phase shifters (d) Optical micrograph of full transmitter PIC.

methods for optimizing a quadrature. When using the integrated PD's, we can interpolate the half-power setting for the I-branch TO phase shifter. When using the received signal, we measure the phase error for the received signal, and adjust the I-branch TO phase shifter until the phase error is minimized.

A summary of the calibration settings can be found in Table II. Currently, we perform the above calibration routines manually on the transmitter test structure. In a future fully-packaged design, however, they will be performed automatically by control algorithms hosted on an integrated FPGA controller.

B. Dynamic Calibration

During transmission, we continue to monitor the power at the monitor PD's. Over time, the statically-calibrated bias points will drift due to thermal and mechanical effects. Using Automatic Bias Control (ABC), we can finely adjust the system bias settings to account for this drift in real time, without interrupting data transmission. To accomplish this, we employ a dither-correlation detection technique similar to [32]. By placing low-speed sine waves of < 100 kHz on top of the control voltages of the child MZM heaters, we can produce a dither signal that can be monitored by the ADC connected to the low-bandwidth monitor PD's.

Our procedure for ABC is as follows. We place a sine wave of frequency f_I on the heater corresponding to $\phi_{I,DC}$, and a sine wave of a different frequency f_Q on the heater corresponding to $\phi_{Q,DC}$. For this ABC technique to work, f_I and f_Q must be distinct and not integer multiples of one another. The interaction of these two signals will produce an intermediate frequency component f_P, equal to the sum of f_I and f_Q. We employ dither-correlation detection at each of the monitor PD's to obtain the correlation integrals for f_I, f_Q, and f_P. We first fine-tune the child MZM DC voltages until their corresponding integrals (f_I and f_Q) at the child PD's have been minimized for phase modulation, or maximized for OOK. Then, we minimize the f_P integral at the parent PD by fine-tuning the DC voltage on the parent MZM. Regardless of format, the appropriate sequence loops for the duration of transmission to maintain system accuracy.

As with the static calibration sequence, ABC will be performed automatically on an integrated FPGA controller in a future packaged design.

VII. FABRICATION AND RESULTS

A. Reconfigurable Transmitter

Our transmitter test structure consists of a complete single-polarization IQ modulator matching the architecture in Fig. 3(b). Fig. 6(a) shows a high-level schematic of the setup we used to test the functionality of this architecture. The transmitter PIC itself was fabricated using an MPW run of TowerJazz Photonics' PH18MC design flow, and then packaged onto a printed circuit board (PCB) with die-attach, DC wirebonding, and fiber-attach (Fig. 6(b)). The TW-MZMs use lateral junction depletion-mode PN phase shifters from the TowerJazz PH18

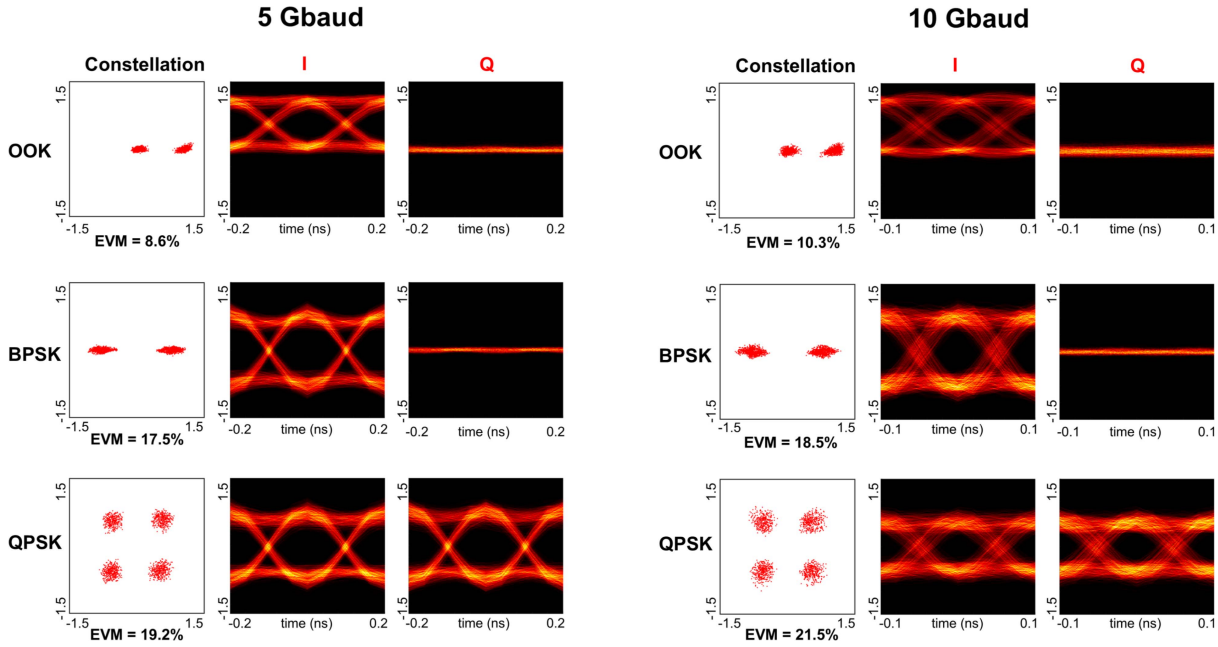

Fig. 7. Constellation and eye diagrams at TX output for OOK, BPSK, and QPSK at 5 and 10 GBaud. Note that the average power for each constellation is normalized to 1.

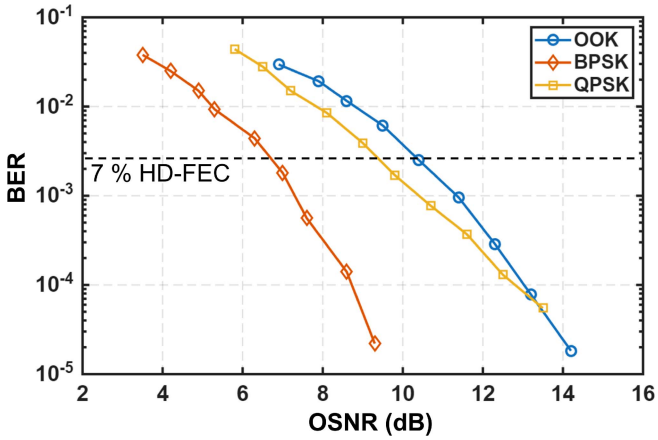

Fig. 8. Transmitter bit-error rate curves for OOK, BPSK, and QPSK at 5 GBaud, referenced to hard-decision FEC limit.

PDK, and the TO phase shifters are made from undercut Titanium Nitride heaters (Fig. 6(c)–(d)). The MZMs are driven with 50 Ω high-speed G-S probes that are connected to a Keysight M9502A arbitrary waveform generator (AWG), which produces inverted and non-inverted signal pairs that are each amplified to 2.4 V_{pp}. The signal pairs are used to drive the TW-MZM's in the push-pull configuration. The data carried by the signal is a $2^{15} - 1$ pseudo-random binary sequence (PRBS-15). A digital-to-analog converter (DAC) is used to send DC control signals to the TO phase shifters, as well as to read current values from the monitor PDs. The modulated optical output from the PIC is then amplified by an Erbium-doped fiber amplifier (EDFA) to maintain a constant signal power of 6 dBm. Finally, it is directed to an Agilent N4391A optical modulation analyzer (OMA) to evaluate the integrity of the signal and capture its spectral characteristics.

To prepare for transmission, we followed the static calibration procedure as described in Table II. We input a 1550 nm optical carrier with a power of 12 dBm through the fiber array, and used the DAC to manually adjust the bias settings to minimize or maximize the PD values as needed for OOK, BPSK, and QPSK. During operation, we measured a pre-amplified optical power of -13 dBm for OOK/BPSK and -16 dBm for QPSK at the PIC output. As shown in Fig. 7, our transmitter successfully generates OOK, BPSK, and QPSK signals at symbol rates up to 10 GBaud. We demonstrate signals with error vector magnitudes (EVM) no greater than 21.5% in all cases. Such performance would enable us to communicate with any of the links in Table I. This EVM value also corresponds to a bit-error rate (BER) well below the 7% overhead hard-decision forward-error correction (FEC) limit for ITU-T G.975.1 compatible FEC ($2.7 * 10^{-3}$). [33]

BER curves versus optical signal to noise ratio (OSNR) were also obtained for the transmitter at 5 GBaud, and can be seen in Fig. 8. The same experimental setup was used, with the addition of a variable optical attenuator (VOA) after the PIC output, and an optical spectrum analyzer in parallel with the OMA in order to measure OSNR. The optical carrier was again a 12 dBm, 1550 nm CW laser. To perform the experiment, the modulator was first biased for a particular modulation format. Then, the VOA was adjusted to obtain various OSNR values, and the BER recorded. This process was repeated for OOK, BPSK, and QPSK. From the results, we observe that all formats can reach the 7% overhead hard-decision FEC limit of $2.7 * 10^{-3}$ at an OSNR of 10.5 dB. The power penalty between BPSK and QPSK at this point is approximately 2.5 dB, and the penalty between BPSK and OOK is 3.5 dB.

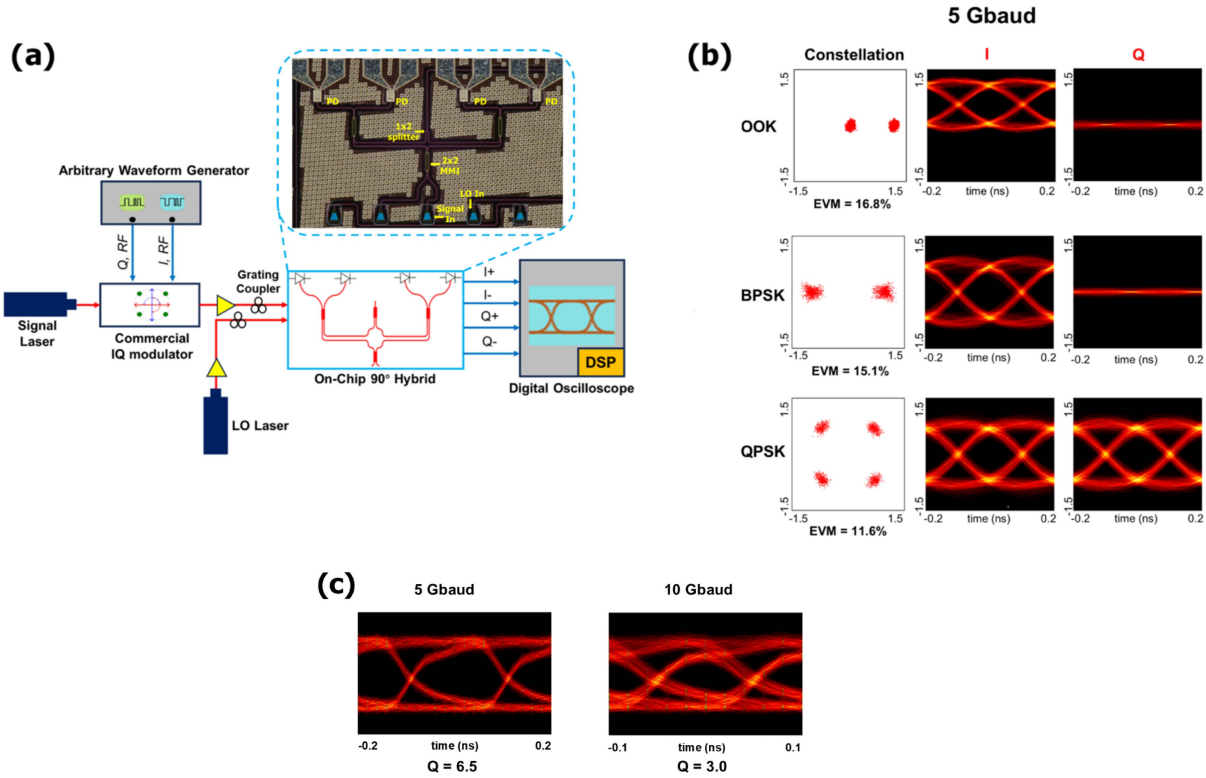

Fig. 9. (a) Full receiver experimental setup with annotated optical micrograph of the 90° hybrid test structure. (b) Constellation and eye diagrams recovered by the RX test structure for OOK, BPSK, and QPSK at 5 GBaud. (c) Eye diagrams with quality factors for direct measurement of OOK at 5 and 10 GBaud.

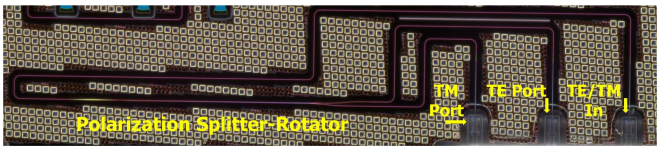

Fig. 10. Annotated optical micrograph of the PSR test structure.

TABLE III
COMPARISON OF SIMULATED AND MEASURED POLARIZATION EXTINCTION RATIOS

	TM ER at TE Port	TE ER at TM Port
Simulation	25 dB	44 dB
Measurement	21.6 dB	35.1 dB

B. Polarization Splitter/Rotator

The PSR test structure consists of an edge-coupled PSR on the test PIC. An optical micrograph of our fabricated design can be seen in Fig. 10.

Test PIC's containing our final design were fabricated in the TowerJazz Photonics PH18MFV process alongside the receiver PIC. 1550 nm CW light from a tunable laser was edge-coupled into the chip via a PM fiber array. A fiber polarization controller was used to pass either TE or TM light exclusively into the device, and an optical power meter (OPM) was used to measure the optical output at each port. Our results are reported in Table III. They show good agreement between simulation and measurement, indicating we will be able to suppress unwanted crosstalk between channels by at least 21 dB. This meets our target of 20 dB, confirming we will have a minimum power penalty on our receiver's sensitivity.

C. Coherent Receiver

Our receiver test structure is a single-polarization 90° hybrid identical to the schematic shown in Fig. 4. The PIC containing this test structure was fabricated using the same full wafer run of the TowerJazz PH18MFV process the PSR test structure was fabricated in. The setup for the experiment characterizing it can be found in Fig. 9(a). We connect to this structure optically via grating couplers, and electrically via 50 Ω high-speed G-S probes. The input signal is generated by an IDPhotonics OMFT-C-00-FA commercial I/Q modulator, which is driven by the Keysight M9502A AWG using a $2^{11} - 1$ PRBS sequence. The signal is placed on a 1549.996 nm optical carrier. The local oscillator is provided by a 1549.990 nm CW laser, leading to an approximately 800 MHz frequency offset. The electrical signals output by the PD's are sent to a Tektronix DPO 72004 digital oscilloscope where the data is exported to MATLAB, where IQ imbalance compensation, frequency offset compensation, clock recovery, constant modulus algorithm (CMA) equalization, and carrier phase recovery is performed to recover the constellations and calculate signal quality. EVM is calculated from the resolved signals.

Currently, we are limited to probing two adjacent RF outputs at a time, such as I_1 and I_2, or I_2 and I_4. The resulting waveforms from the oscilloscope can be seen in Fig. 9(b). We can see that

TABLE IV
COMPARISON OF PUBLISHED RECONFIGURABLE AND MULTI-FORMAT COHERENT TRANSCEIVERS

Work	TX/RX	Polarization	Formats Demonstrated	Max Baud Rate
[34]	TX + RX	Single	BPSK, QPSK	5 GBaud
[35]	TX	Single	QPSK, 16-QAM	28 GBaud (QPSK) 20 GBaud (16-QAM)
[36]	TX	Single Dual (OOK and BPSK only)	OOK, BPSK, QPSK, PAM-4	10 GBaud
This Work	TX + RX	Dual	OOK, BPSK, QPSK	10 GBaud (TX) 5 GBaud (RX)

our 90° hybrid can successfully resolve OOK, BPSK, and QPSK up to 5 GBaud after applying standard DSP techniques. For each format, the EVM never exceeds 16.8%. Currently, this is compatible with our transmitter and most of the links in Table I.

By only measuring adjacent channels, we were unable to use both PD's per channel to remove the signal, LO, and noise beating terms, preventing measurement of QPSK at higher Baud rates. [28] To verify that our receiver can scale to the higher Baud rates supported by the transmitter, we performed direct detection of the OOK signal at 5 and 10 GBaud using only the I_2 channel. For this experiment, we used the aforementioned setup, but did not send the local oscillator into the structure. I_2 alone was sent into the digital oscilloscope, where the eye diagram could be directly recovered. These eye diagrams and measured quality-factors can be seen in Fig. 9(c). We can see that the signal can indeed be received by this 90° hybrid structure at 10 GBaud, verifying that we are limited by the probing setup, and not by the architecture itself. In the future, we will attempt to probe I_1, I_2, I_3, and I_4 at the same time in order to resolve data at higher Baud rates for all format types.

VIII. CONCLUSION AND FUTURE WORK

As demonstrated, our architecture compares favorably with those from the literature, which can seen in Table IV. To our knowledge, this work presents the first demonstration of a fully reconfigurable, polarization-multiplexed Si photonic transceiver architecture supporting both coherent and direct detection schemes. We successfully demonstrated transmission for OOK, BPSK, and QPSK at 10 GBaud, reception at 5 GBaud, and low-crosstalk on-chip polarization multiplexing. In each case, the signal BER was below the 7% hard-decision forward-error correction (FEC) limit of $2.7 * 10^{-3}$. Critically, this transceiver is entirely compatible with standard SOI photonic foundry processes and can be fabricated using PDK components, making it highly scalable for mass production with high yield.

Future efforts will focus on refining the device-level designs to support even higher bandwidths, while also achieving compatibility with CMOS electronic drivers. We are currently constructing a fully integrated system, the core of which will be a PIC featuring the complete transceiver (transmit and receive), with both polarization channels present, all on one chip. This PIC is designed for direct integration with a custom-designed EIC containing the RF drivers, bias control circuitry, and TIA's for the photodiode outputs. The EIC will then connect to a DSP chip that performs the necessary operations to recover the received signal. This chip package will be controlled from a central FPGA, running the appropriate bias control algorithms and handling the data streams for transmit and receive. In designing for a practical OISL, it will be necessary to carefully choose a DSP implementation that balances the tradeoffs of overhead, latency, and power consumption. A choice of hard-decision FEC, soft-decision FEC, or a concatenation of the two will depend on the acceptable overhead in a given circumstance, as modern standards like OIF 800LR lower power consumption and latency in exchange for high overheads over 21%. [37] In general, soft-decision FEC is most responsible for increasing overhead. [38] We will also ensure use of a low-linewidth laser, as a narrower linewidth allows for a longer averaging span for phase estimation, reducing the BER penalty from phase error correction. [28]

The key enabling device for CMOS-compatible transmission will be a custom-designed segmented-electrode TW-MZM. This MZM will use a differential-driver scheme, where a signal is applied to the cathode of the phase shifter diode at the same time its inverse is applied to the anode. Distinct DC biases are also applied to each side of the junction. This allows us to increase the possible voltage swing from the 1.4 V_{pp} of each EIC channel to a 2.8 V_{pp} maximum differential swing. When combined with a push-pull configuration for the arms of the MZM, we can obtain the full range of phase shifts required (Fig. 3(d)) using CMOS drivers on a standard silicon platform. Splitting the phase shifter into two identical segmented electrodes [39] will enable us to drive only half the length of the TW-MZM with an individual EIC channel, improving the RF bandwidth of the device. With this design, we aim to achieve 20 GBaud operation in a CMOS-driven package.

A further benefit of the transmitter and receiver sharing a single PIC is the ability to integrate adaptive DSP techniques that run in real time [40] in order to further improve EVM and overall signal fidelity. Internal loopbacks have been designed to connect the transmitter and receiver on-chip in order to measure nonidealities that then can be digitally pre-compensated. Some examples of compensation algorithms that can be run include clock recovery, equalization, frequency and phase recovery, and demodulation. Additionally, this fully-packaged architecture will enable further static calibration to compensate for specific device variations, both for the transmitter and the receiver. For example, a power imbalance between I and Q can be detected, and compensated by increasing the RF driver power of the weaker signal. Similarly, we can implement digital de-skew by delaying I or Q if they are out of phase electrically. Antidroop and Digital Pre Distortion (DPD) filters can also be characterized and applied to obtain a flat optical power response vs frequency and electrical input drive, respectively. Through the

use of DPD, we can adjust the linearity of the transmitter to reliably enable multi-amplitude modulation formats, including PAM-4 and 16-QAM. These formats are compatible with our existing architecture and its static calibration routines. PAM-4 and 16-QAM can be obtained by setting the MZM to OOK and QPSK, respectively, and sending four-level electrical signals to the electro-optic modulators. In this way, our architecture can be easily scaled to support higher-order modulation formats, allowing it to continue to accommodate the evolving satellite communication environment.

The fully-packaged unit will be intended for use in LEO satellites. As such, in addition to the calibration routines compensating for thermal fluctuations, vibrations, and propagation losses, the unit will also need to consider radiation-hardness. Radiation primarily damages PIC's through waveguide oxidation (increases loss and changes effective index) and changes in carrier concentration (increases dark current and changes PN junction behavior). [41], [42] The package will therefore also possess the responsibility of minimizing the ionizing dose for the PIC and electrical chips. [43] demonstrated that several mm of aluminum shielding can block almost all electron radiation, most solar flare particles, and a large portion of the protons seen in LEO. Further investigations into radiation hardness can be conducted using the methods described in [43].

Ultimately, this unit will serve as a low-latency, high-throughput reconfigurable OISL, enabling inter-satellite connectivity for dense LEO constellation formations.

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